UM1521
User manual

STM32L152D-EVAL evaluation board

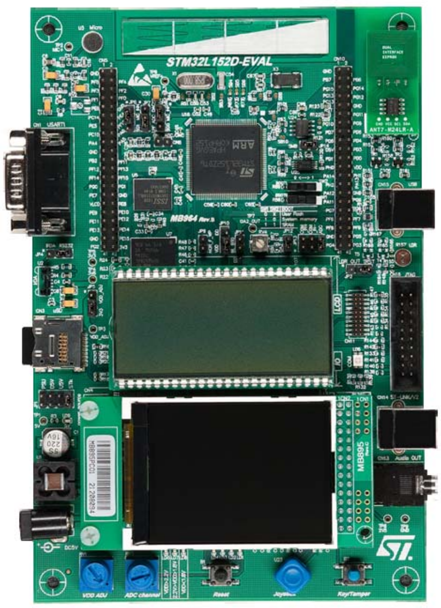
Introduction

The STM32L152D-EVAL evaluation board is a complete demonstration and development platform for the ARM Cortex-M3 core-based STM32L152ZDT6 microcontroller from STMicroelectronics featuring two I2Cs, three SPIs, five USARTs, 12-bit ADC, 12-bit DAC, LCD driver, internal 48 KB SRAM and 384 KB Flash, touch sensing, USB FS, LCD controller, FSMC and JTAG debugging support.

This board can be used as reference design for user application development but it is not considered as final application. The full range of hardware features on the board helps you evaluate all peripherals (USB FS, USART, audio DAC, microphone ADC, dot-matrix LCD, LCD glass, IrDA, LDR, SRAM, NOR Flash, MicroSD Card, temperature sensor and so on) and develop your own applications. Extension headers make it possible to easily connect a daughterboard or wrapping board for your specific application.

An ST-LINK/V2 is integrated on the board as embedded in-circuit debugger and programmer for the STM32 MCU.

Figure 1. STM32L152D-EVAL evaluation board



This user manual applies to the products listed in *Table 1*.

Table 1. Applicable tools

Type	Part numbers
Evaluation tools	STM32L152D-EVAL

Contents

1 Overview

1.1 Features

- Four 5 V power supply options: Power jack, ST-LINK/V2 USB connector, user USB connector or daughterboard
- Audio jack connected to I2S DAC, or STM32L152ZDT6 internal DAC
- Microphone connected to ADC using integrated op amp as amplifier
- 2 GByte (or more) MicroSD Card on SDIO interface
- Temperature sensor and RF EEPROM on I2C compatible serial interface
- RS-232 interface configurable for communication or Flashloader
- IrDA transceiver
- JTAG and trace debug support, embedded ST-LINK/V2
- 4 Kbit serial Flash, 512K x16-bit SRAM and 128 Mbit NOR Flash
- 240x320 TFT color LCD connected to FSMC interface of STM32L152ZDT6
- Joystick with 4-direction control and selector
- Reset and Tamper or key button
- 4 color user LEDs and 3 LEDs as MCU power range indicator
- MCU consumption measurement circuit
- LCD glass 40 x 8 segments connected to LCD driver of STM32L152ZDT6
- Extension connector for daughterboard or wrapping board
- MCU voltage choice of 3.3 V or adjustable from 1.65 V to 3.6 V
- USB FS connector
- Touch slider
- Light dependent resistor (LDR)
- One MCU integrated op amp configured as Sallen-Key 2nd order low pass filter
- One MCU integrated op amp configured as amplifier with adjustable gain
- One ADC / DAC input signal connector
- Potentiometer

1.2 Demonstration software

Demonstration software is preloaded in the board's Flash memory for easy demonstration of the device peripherals in stand-alone mode. For more information and to download the latest version available, please refer to the STM32L152D-EVAL demonstration software available on www.st.com.

1.3 Order code

To order the STM32L152ZDT6 evaluation board, use the order code STM32L152D-EVAL.

1.4 Delivery recommendations

Some verifications are needed before using the board for the first time to make sure that nothing was damaged during shipment and that no components are unplugged or lost.

When the board is extracted from its plastic bag, please check that no component remains in the bag.

The main components to verify are:

1. The 8 MHz crystal (X1) which may have been removed by a shock from its socket.
2. The MicroSD Card which may have been ejected from the connector CN3 (left side of the board).
3. The dual-interface EEPROM board (ANT7-M24LR-A) which may have been unplugged from the connector CN12 (top right corner of the board).

2 Hardware layout and configuration

The STM32L152D-EVAL evaluation board is designed around the STM32L152ZDT6 (144-pin TQFP package). The hardware block diagram *Figure 2* illustrates the connection between STM32L152D-EVAL and peripherals (LCD glass, Color LCD, Touch slider, USB FS connector, Temperature Sensor, USART, IrDA, Audio, SRAM, Nor Flash, EEPROM,RF EEPROM, MicroSD Card and embedded ST-LINK) and *Figure 3* will help you locate these features on the actual evaluation board.

Figure 2. Hardware block diagram

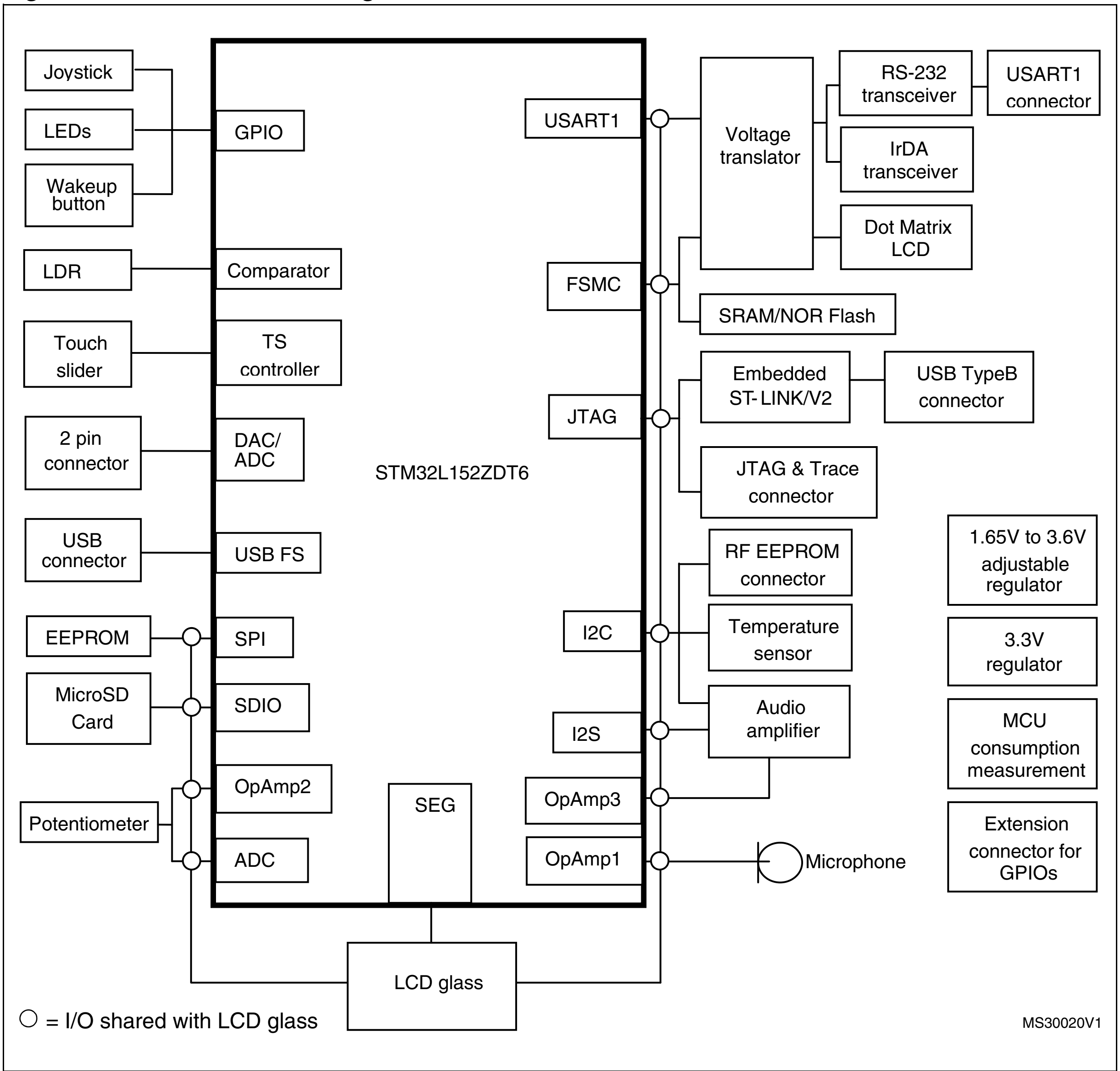
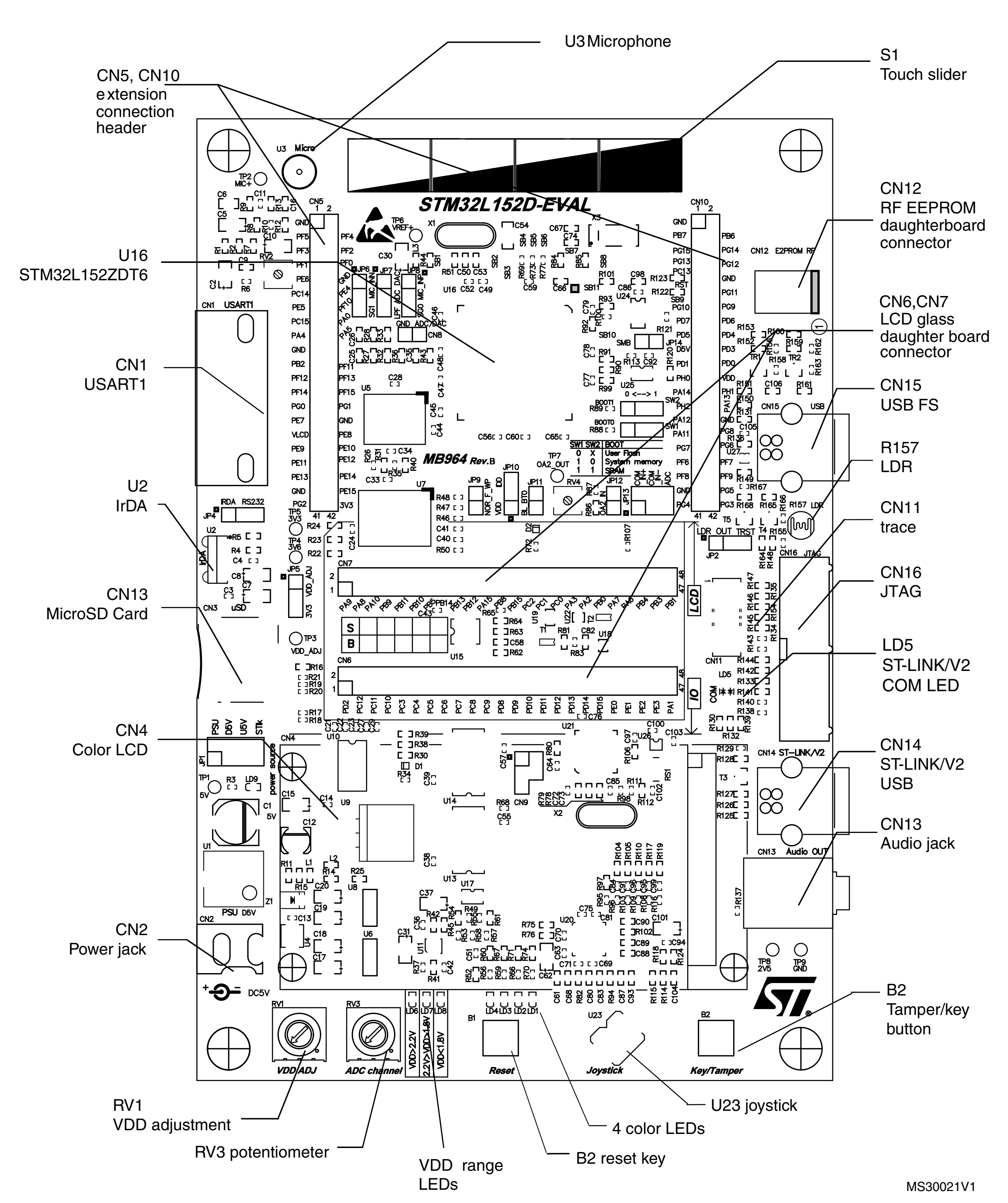


Figure 3. Hardware block diagram



2.1 Development and debug support

Version 2 of the ST-LINK called ST-LINK/V2 is embedded on the board. This tool allows program loading and debugging on the STM32L using a JTAG or SWD interface. Third-party debug tools are also supported by JTAG connector CN16 and Trace connector CN11.

A specific driver must be installed on your PC for communication with embedded ST-LINK/V2. To download and install this driver, use the install shield called ST-LINK_V2_USBdriver.exe available on the Software and development tools page for ultra low power STM32L family available on www.st.com.

Third-party toolchains support ST-LINK/V2 according to *Table 2*.

Table 2. Third party support of ST-LINK/V2

Third party	Toolchain	Version
Atollic	TrueSTUDIO	2.1
IAR	EWARM	6.20.4
Keil	MDK-ARM	4.20
Tasking VX-Toolset	ARM Cortex-M	4.0.1

The embedded ST-LINK/V2 is connected to the PC via a standard USB cable connected to connector CN14. The bicolor LED LD5 (COM) advises on the communication status as follows:

- Slow blinking Red LED/Off: At power on before USB initialization.
- Fast blinking Red LED/Off: After the first correct communication between PC and ST-LINK/V2 (enumeration).
- Red LED On: When initialization between PC and ST-LINK/V2 is successfully finished.
- Green LED On: After successful target communication initialization.
- Blinking Red/Green LED: During communication with target.
- Red LED On: Communication finished and OK.
- Orange LED On: Communication failure.

Note: It is possible to power the board via CN14 (embedded ST/LINK/V2 USB connector) even if an external tool is connected to CN11 (Trace connector) or CN16 (external JTAG & SWD connector).

2.2 Power supply

The STM32L152D-EVAL evaluation board is designed to be powered by a 5 V DC power supply and to be protected by PolyZen from a wrong power plug-in event.

It is possible to configure the evaluation board to use any of following four sources for the power supply.

- 5 V DC power adapter connected to CN2, the power jack on the board (power supply unit (PSU) on silkscreen). The external power supply is not provided with the board.
- 5 V DC power with 500mA limitation from CN14, the USB type B connector of ST-LINK/V2 (USB 5 V power source on silkscreen (ST-LINK/V2)).
- 5 V DC power with 500mA limitation from CN15, the USB type B connector (USB 5V power source on silkscreen (USB)).
- 5 V DC power from CN10, the extension connector for daughterboard (daughterboard power source on silkscreen (D5V)).

The LEDs indicate the following:

- LED LD9 is lit when the STM32L152D-EVAL board is powered by 5 V correctly.
- Red LED LD8 is lit when the MCU is powered by low voltage (VDD < 1.8 V).
- Yellow LED LD7 is lit when the MCU is powered by voltage (1.8 V < VDD < 2.2 V).
- Green LED LD6 is lit when the MCU is powered by voltage (2.2 V < VDD).

The power supply is configured by setting the related jumpers JP1, JP5 and JP10 as described in *Table 3*.

Table 3. Power supply jumper settings

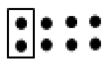
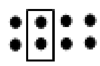
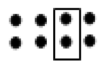
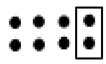
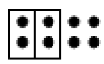
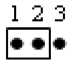
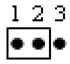
Jumper	Description	Setting
JP1	JP1 selects one of the four possible power supply sources.	
	– For power supply jack(CN2) to the STM32L152D-EVAL only, JP1 is set as shown to the right:	PSU D5V U5V STK 
	– For power supply from the daughterboard connectors (CN10) to STM32L152D-EVAL only, JP1 is set as shown to the right:	
	– For power supply from USB (CN15) to STM32L152D-EVAL only, JP1 is set as shown to the right:	
	– For power supply from USB connector of ST-LINK/V2 (CN14) to STM32L152D-EVAL only, JP1 is set as shown to the right: (**Default setting**)	
	For power supply from power supply jack (CN2) to both STM32L152D-EVAL and daughterboard connected on CN5 and CN10, JP1 is set as shown to the right (daughterboard must not have its own power supply connected)	

Table 3. Power supply jumper settings (continued)

Jumper	Description	Setting
JP5	VDD is connected to fixed +3.3 V DC power when JP5 is set as shown to the right: (**Default setting**)	
	VDD is connected to adjustable DC power from 1.65 V to 3.6 V when JP5 is set as shown to the right:	
JP10	VDD power is directly connected to MCU VDD when JP10 is set as shown to the right (**Default setting**): Note: For manual I_{DD} measurement the jumper on JP10 must be removed and replaced by an ammeter connected between pin 1 and 2 of JP10.	
	Connect VDD power to MCU with current-sampling resister, 1 Ohm or 1 KOhm, in series for I_{DD} current measurement when JP10 is set as shown to the right:	

Note: *Due to some peripheral component specifications, the low voltage limitations (component will not work correctly when power level is under low voltage limitation) related to the operating voltage of the peripherals are shown in Table 4.*

Table 4. Low voltage limitation

Peripheral	Component	I/O name	Low voltage limitation
USB	CN15	USB	3 V
MicroSD Card	CN3	SDIO	2.7 V
SRAM	U5	FSMC	2.4 V
EEPROM	U25	SPI	1.8 V
RF EEPROM	CN12	I2C	1.8 V

Note: *The recommended AC220 V to DC5 V power adapter is the PSU-5V2A. It is not included with the board but can be ordered from ST as a separate item. You can also use another equivalent 5 V power adapter (polarity compatible with CN2) to power the STM32L152D-EVAL board via the CN2 power jack on the board.*
To order the recommended power supply, use the order code PSU-5V2A.

2.3 Clock source

Two clock sources are available on the STM32L152D-EVAL evaluation board for the STM32L152ZDT6 and RTC embedded.

- X1, 8 MHz crystal with socket for the STM32L152ZDT6 microcontroller, it can be removed from socket when internal RC clock is used.
- X3, 32 kHz crystal for embedded RTC

Table 5. 8 MHz crystal X1 related solder bridges

Solder bridge	Description
SB1	PH1 is connected to 8 MHz crystal when SB1 is open. (**Default setting**)
	PH1 is connected to extension connector CN10 when SB1 is closed. In such case R51 must be removed to avoid disturbance due to the 8Mhz quartz
SB2	PH0 is connected to 8 MHz crystal when SB2 is open. (**Default setting**)
	PH0 is connected to extension connector CN10 when SB2 is closed. In such case C53 and X1 must be removed.

Table 6. 32 kHz crystal X3 related solder bridges

Solder bridge	Description
SB8	PC14 is connected to 32 kHz crystal when SB8 is open. (**Default setting**)
	PC14 is connected to extension connector CN5 when SB8 is closed. In such case R85 must be removed to avoid disturbance due to the 32kHz quartz
SB7	PC15 is connected to 32 kHz crystal when SB7 is open. (**Default setting**)
	PC15 is connected to extension connector CN5 when SB7 is closed. In such case R84 must be removed to avoid disturbance due to the 32 kHz quartz

2.4 Reset source

The reset signal of the STM32L152D-EVAL evaluation board is low active and the reset sources include:

- Reset button B1
- Debug tools from JTAG connector CN16 and trace connector CN11
- Daughterboard from CN10
- Embedded ST-LINK/V2
- RS-232 connector CN1 for ISP

2.5 Boot option

The STM32L152D-EVAL evaluation board is able to boot from:

- Embedded user Flash
- System memory with boot loader for ISP
- Embedded SRAM for debugging

The boot option is configured by setting switch SW1 (BOOT0) and SW2 (BOOT1). The BOOT0 can be configured also via the RS-232 connector CN1.

Table 7. Boot related switch

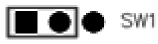
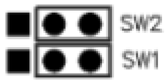
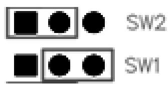
Switch	Boot from	Switch configuration
SW1 and SW2	STM32L152D-EVAL boots from user Flash when SW1 is set as shown to the right. SW2 is don't care in this configuration. (**Default setting**)	0 <----> 1 
	STM32L152D-EVAL boots from embedded SRAM when SW1 and SW2 are set as shown to the right.	0 <----> 1 
	STM32L152D-EVAL boots from system memory when SW1 and SW2 are set as shown to the right.	0 <----> 1 

Table 8. Boot0 related jumpers

Jumper	Description
JP11	The Bootloader_BOOT0 is managed by pin 6 of connector CN1 (RS-232 DSR signal) when JP11 is closed. This configuration is used for boot loader application only. **Default setting**: Not fitted

2.6 LCD glass module

An LCD glass module daughterboard (MB979) is mounted on the STM32L152D-EVAL evaluation board. It can be connected to the LCD driver of the STM32L152ZDT6 or work as a set of jumpers by mounting it on two possible positions; position "IO" or position "LCD":

- When the LCD glass module is mounted on position IO (see *Figure 4*), all peripherals (memories, USART, audio, EEPROM, potentiometer, MicroSD Card, microphone, etc) shared with the LCD glass are connected to the STM32L152ZDT6, and the LCD glass is disconnected (default setting).
- When the LCD glass module is mounted on position LCD (see *Figure 5*), the LCD glass is connected to the LCD driver of the STM32L152ZDT6 and all peripherals shared with LCD glass are disconnected.

Figure 4. Position IO

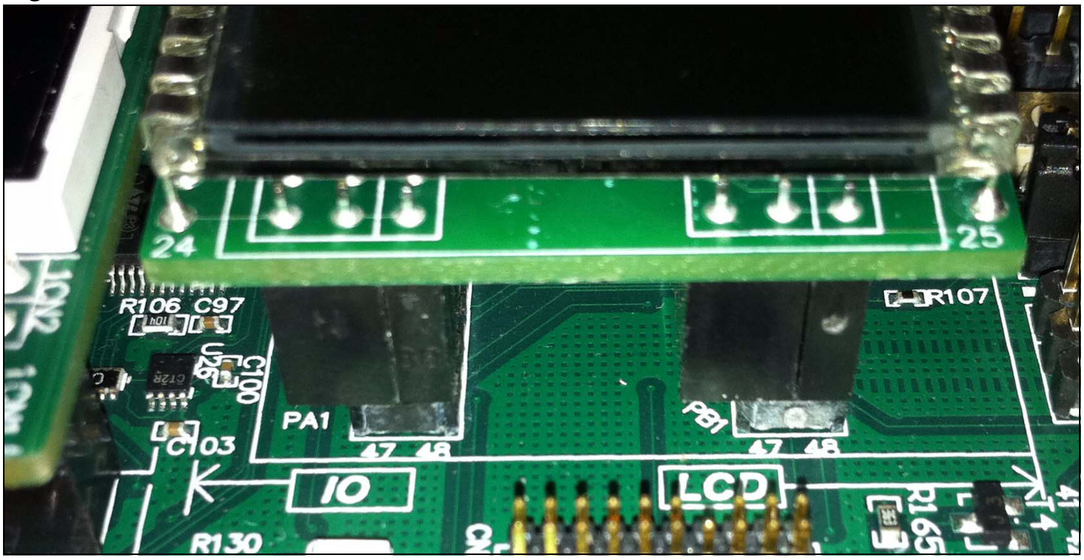


Figure 5. Position LCD

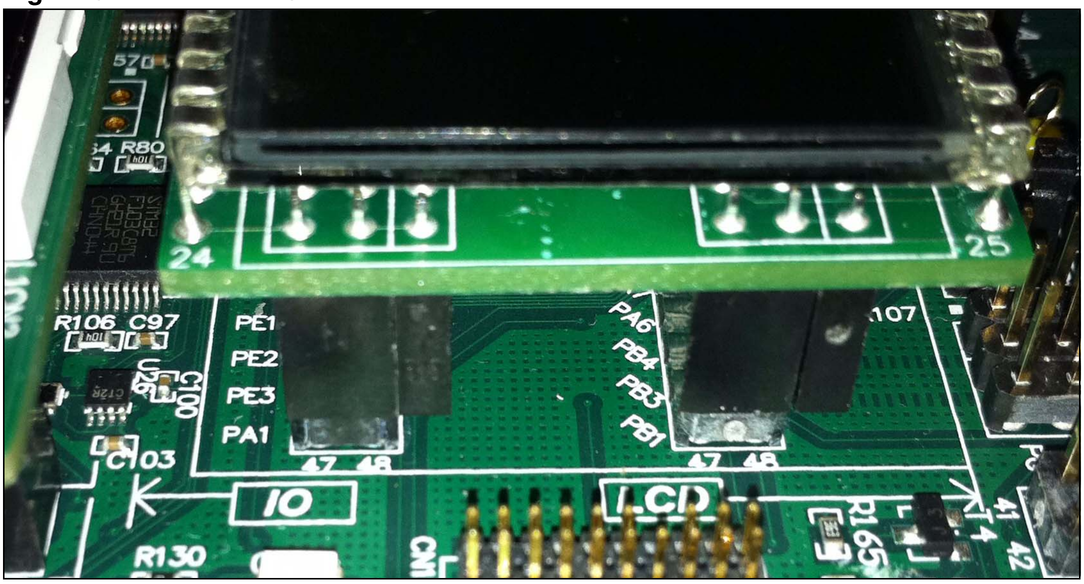
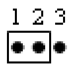
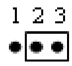
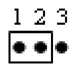
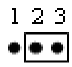


Table 9. **LCD glass related jumpers**

Jumper	Description	Setting
JP8	PA1 is connected to microphone (MIC_INP signal) when JP8 is set as shown to the right: (**Default setting**)	
	PA1 is connected to LCD glass as SEG0 when JP8 is set as shown to the right:	
JP6	PA2 is connected to microphone (MIC_INN signal) when JP6 is set as shown to the right: (**Default setting**)	
	PA2 is connected to LCD glass as SEG1 when JP6 is set as shown to the right:	

The custom LCD glass on MB979 is model XHO5002B. The signal mapping is shown in *Table 10*, *Table 11*, *Table 12* and *Table 13* and segment names are given in *Figure 6*.

Table 10. **LCD glass segments mapping table pins 1-12**

Pin	1	2	3	4	5	6	7	8	9	10	11	12
COM1	COM1				1g	2g	3g	4g	5g	6g	7g	8g
COM2		COM2			1h	2h	3h	4h	5h	6h	7h	8h
COM3			COM3		1i	2i	3i	4i	5i	6i	7i	8i
COM4				COM4	1j	2j	3j	4j	5j	6j	7j	8j
COM5					1d	2d	3d	4d	5d	6d	7d	8d
COM6					1c	2c	3c	4c	5c	6c	7c	8c
COM7					1e	2e	3e	4e	5e	6e	7e	8e
COM8					1f	2f	3f	4f	5f	6f	7f	8f

Table 11. **LCD glass segments mapping table pins 13-24**

Pin	13	14	15	16	17	18	19	20	21	22	23	24
COM1	9g	10g	11g	12g	13g	14g	15g	16g	17g	18g	19g	5J
COM2	9h	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h	5C
COM3	9i	10i	11i	12i	13i	14i	15i	16i	17i	18i	19i	5B
COM4	9j	10j	11j	12j	13j	14j	15j	16j	17j	18j	19j	5I
COM5	9d	10d	11d	12d	13d	14d	15d	16d	17d	18d	19d	13a
COM6	9c	10c	11c	12c	13c	14c	15c	16c	17c	18c	19c	13b
COM7	9e	10e	11e	12e	13e	14e	15e	16e	17e	18e	19e	O1
COM8	9f	10f	11f	12f	13f	14f	15f	16f	17f	18f	19f	O2

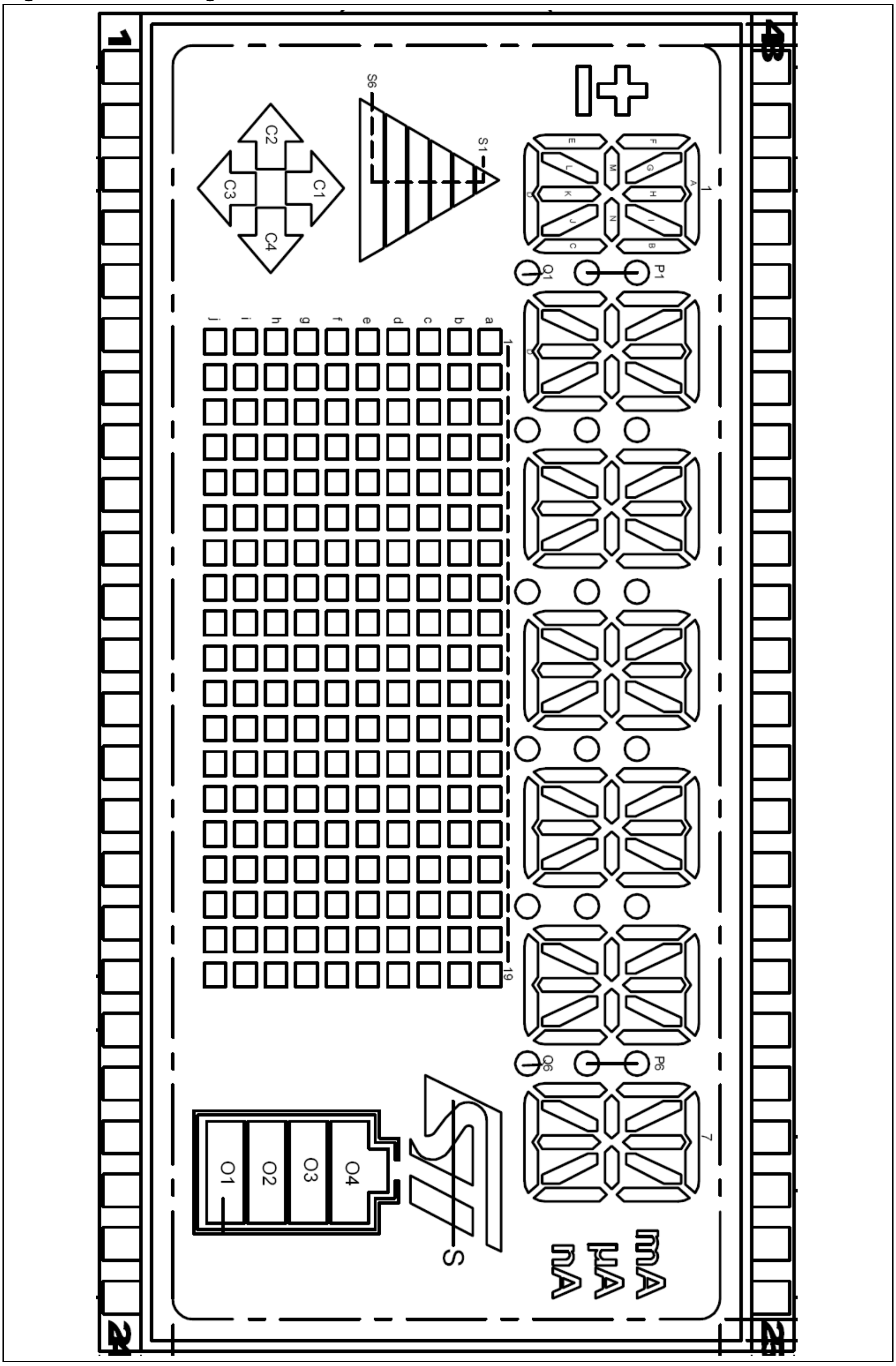
Table 12. LCD glass segments mapping table pins 25-36

Pin	25	26	27	28	29	30	31	32	33	34	35	36
COM1	7J	7N	7E	6J	6N	6E	5N	5E	4J	4N	4E	3J
COM2	7C	7M	P6	6C	6M	P5	5M	P4	4C	4M	P3	3C
COM3	7B	7H	7F	6B	6H	6F	5H	5F	4B	4H	4F	3B
COM4	7I	7A	7G	6I	6A	6G	5A	5G	4I	4A	4G	3I
COM5	19a	18a	17a	16a	15a	14a	12a	11a	10a	9a	8a	7a
COM6	19b	18b	17b	16b	15b	14b	12b	11b	10b	9b	8b	7b
COM7	S	7D	Q6	O4	6D	Q5	5D	Q4	µA	4D	Q3	C4
COM8	nA	7K	7L	O3	6K	6L	5K	5L	mA	4K	4L	C3

Table 13. LCD glass segments mapping table pins 37-48

Pin	37	38	39	40	41	42	43	44	45	46	47	48
COM1	3N	3E	2J	2N	2E	1J	1N	1E				
COM2	3M	P2	2C	2M	P1	1C	1M	+				
COM3	3H	3F	2B	2H	2F	1B	1H	1F				
COM4	3A	3G	2I	2A	2G	1I	1A	1G				
COM5	6a	5a	4a	3a	2a	1a	S3	S1	COM5			
COM6	6b	5b	4b	3b	2b	1b	S4	S2		COM6		
COM7	3D	Q2	C1	2D	Q1	S5	1D	-			COM7	
COM8	3K	3L	C2	2K	2L	S6	1K	1L				COM8

Figure 6. LCD segment names

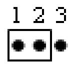
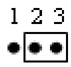


2.7 Audio

The STM32L152D-EVAL evaluation board supports stereo audio play by using an audio DAC CS43L22 connected to both I2S2 port and one channel of DAC in the microcontroller STM32L152ZDT6.

- OpAmp3 of the STM32L152ZDT6 acts as a low pass filter of audio output for this DAC.
- A headphone jack is connected to the output of CS43L22.
- A microphone is connected to ADC through OpAmp1 of STM32L152ZDT6.

Table 14. Audio related jumpers

Jumper	Description	Setting
JP7	PA4 is connected to analog input signal for ADC or output signal from DAC on CN8 when JP7 is set as shown to the right:	
	PA4 output signal to OpAmp3 as low pass filter when JP7 is set as shown to the right: (**Default setting**)	
JP8	Description of JP8 is in *Section 2.6: LCD glass module*	
JP6	Description of JP6 is in *Section 2.6: LCD glass module*	

The I2C address of CS43L22 is 0b1001010.

The LCD glass module has to be mounted on "IO" position for Audio I2C usage. Refer to *Section 2.6: LCD glass module* for detail.

2.8 USB

The STM32L152D-EVAL evaluation board supports USB2.0 compliant full speed communication via a USB type B connector (CN15). The evaluation board can be powered by this USB connection at 5 V DC with a 500 mA current limitation.

USB disconnection simulation can be implemented by controlling the internal 1.5 K pull-up resistor on USB+ line and detection of 5 V power on USB connector CN15 by using a resistor bridge connected to PE6.

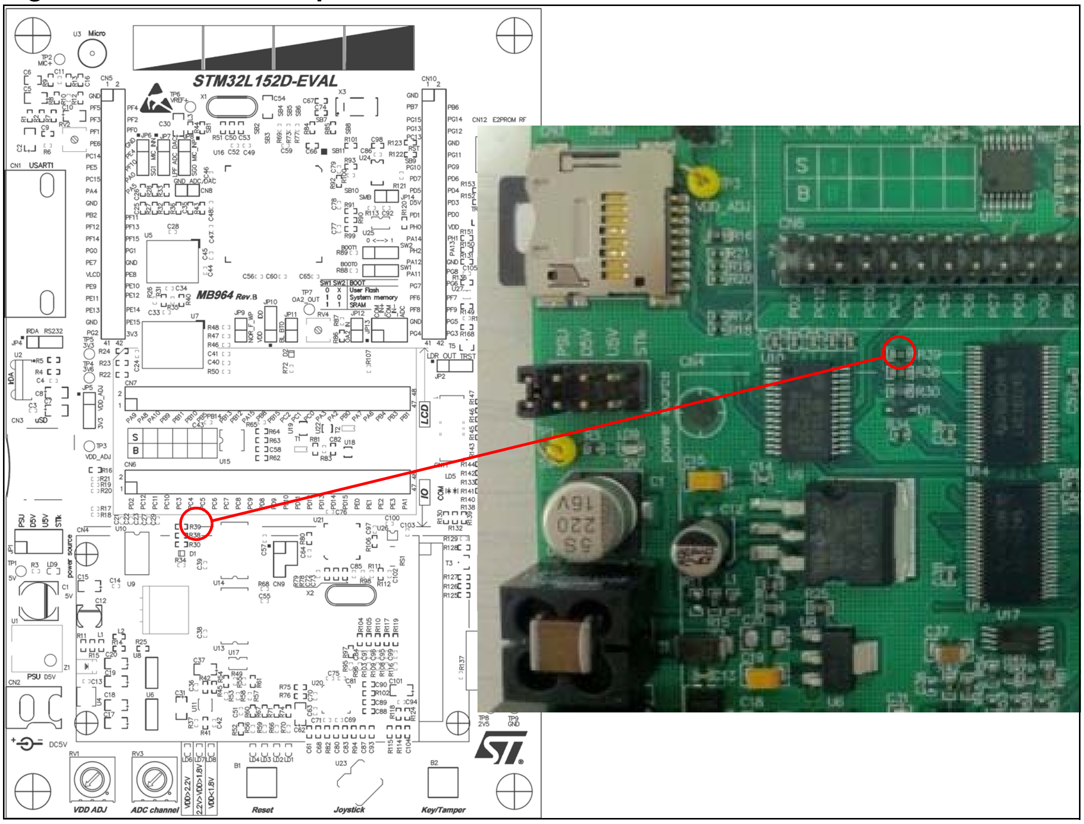
USB will work properly when VDD > 3 V.

2.9 RS-232 and IrDA

RS-232 and IrDA communication is supported by D-type 9-pin RS-232 connector CN1, and IrDA transceiver U2 which is connected to USART1 of the STM32L152ZDT6 on the STM32L152D-EVAL evaluation board.

The signals Bootloader_RESET and Bootloader_BOOT0 can be added on RS-232 connector CN1 for ISP support. If Bootloader_RESET signal is used, mount R39 (Default: Unmounted) with a 0 Ohm resistor as *Figure 7* shows.

Figure 7. R39 resistor placement



Note: If Bootloader_RESET signal is not used, remove R39 to avoid disturbance due to CTS signal from pin8 of CN1, which could cause MCU reset with some software.

Table 15. RS-232 & IrDA related jumpers

Jumper	Description	Setting
JP4	USART1_RX is connected to RS-232 transceiver and RS-232 communication is enabled when JP4 is set as shown to the right (**Default setting**):	1 2 3 (2-3)
	USART1_RX is connected to IrDA transceiver and IrDA communication is enabled when JP4 is set as shown to the right:	1 2 3 (1-2)

The LCD glass module has to be mounted on IO position for USART1 usage. Refer to *Section 2.6: LCD glass module* for detail.

2.10 Touch sensing slider

The STM32L152D-EVAL evaluation board supports a touch sensing slider based on either RC charging or charge transfer technology. The charge transfer technology is enabled by default assembly.

PB6 and PB7 manage an active shield reducing sensitivity to other signals. The active shield is placed on an internal layer immediately under the slider (layer 2) to cover components related to the slider and the slider itself.

Table 16. Touch sensing slider related solder bridges

Solder bridge	Description
SB3	PF9 is connected to sampling capacitor when SB3 is open. (**Default setting**)
	PF9 is connected to extension connector CN10 when SB3 is closed. In this case C54 must be removed to avoid disturbance due to the capacitor
SB4	PF8 is connected to touch slider when SB4 is open. (**Default setting**)
	PF8 is connected to extension connector CN10 when SB4 is closed. In this case R69 must be removed to avoid disturbance due to the touch slider
SB5	PF7 is connected to touch slider when SB5 is open. (**Default setting**)
	PF7 is connected to extension connector CN10 when SB5 is closed. In this case R73 must be removed to avoid disturbance due to the touch slider
SB6	PF6 is connected to touch slider when SB6 is open. (**Default setting**)
	PF6 is connected to extension connector CN10 when SB6 is closed. In this case R77 must be removed to avoid disturbance due to the touch slider
SB10	PB6 is connected to touch slider when SB10 is open. (**Default setting**)
	PB6 is connected to extension connector CN10 when SB10 is closed. In this case R92 must be removed to avoid disturbance due to the shield
SB11	PB7 is connected to touch slider when SB11 is open. (**Default setting**)
	PB7 is connected to extension connector CN10 when SB11 is closed. In this case R101 must be removed to avoid disturbance due to the capacitor

Note: The slider is optimized when the board is powered at 3.3 V. It may be necessary to adjust the capacitor value of C54 (47nF COG) and the firmware to adapt them to a low voltage.

2.11 MicroSD Card

The 2 GB (or more) MicroSD Card connected to the SDIO port of the STM32L152ZDT6 is available on the board. MicroSD Card detection is managed by standard I/O port PC7.

The MicroSD Card will work properly when VDD > 2.7 V.

The LCD glass module has to be mounted on IO position for MicroSD Card usage. Refer to *Section 2.6: LCD glass module* for detail.

2.12 Serial EEPROM

A 4 Kbit (M95040-R) serial EEPROM is connected to SPI1 of the STM32L152ZDT6.

Serial Flash chip select is managed by I/O pin PB0.

The EEPROM will work properly when VDD > 1.8 V.

The LCD glass module has to be mounted on IO position for SPI EEPROM usage. Refer to *Section 2.6: LCD glass module* for detail.

2.13 RF EEPROM

The RF EEPROM daughterboard (MB1020) implemented on the module is the M24LR64-R. This EEPROM can be accessed by the MCU via the I2C bus or by RF using a 13.56 MHz reader (for instance CR95HF).

The daughterboard can be connected to the STM32L152ZDT6 via the I2C bus on CN2.

The I2C address of RF EEPROM is 0b1010E2E1E0. E0-E2 values are determined by the RF EEPROM daughterboard.

The RF EEPROM will work properly when VDD > 1.8 V.

The LCD glass module has to be mounted on IO position for RF EEPROM usage. Refer to *Section 2.6: LCD glass module* for detail.

2.14 SRAM

512Kx16-bit SRAM is connected to bank2 of the FSMC interface and both 8-bit and 16-bit accesses are allowed by BLN0 and BLN1 connected to BLE and BHE of SRAM respectively.

The SRAM will work properly when VDD > 2.4 V.

The LCD glass module has to be mounted on IO position for SRAM usage. Refer to *Section 2.6: LCD glass module* for detail.

2.15 NOR Flash

128 Mbit NOR Flash is connected to bank1 of the FSMC interface. The 16-bit operation mode is selected by pull-up resister connected to BYTE pin of NOR Flash. Write protection is enabled or disabled by jumper JP9.

Table 17. NOR Flash related jumpers

Jumper	Description
JP9	Write protection is enabled when JP9 is fitted while write protection is disabled when JP9 is not fitted. **Default setting**: Not fitted

The LCD glass module has to be mounted on IO position for NOR Flash usage. Refer to *Section 2.6: LCD glass module* for detail.

2.16 Analog input

A 2-pin connector, CN8, is connected to PA4 of the STM32L152ZDT6 as an external analog input or DAC output. A low pass filter can be implemented for a 2-pin connector by replacing R43 and C35 with ADC input or replacing R36 and C35 with DAC output, with correct values of resistor and capacitor as requested by end user's application.

There are also three analog signals available on the board:

1. 10 KOhm potentiometer RV3 connected to PF10.
2. 10 KOhm potentiometer RV3 connected to OpAmp2 PA6.
3. I_{DD} measurement output signal connected to PF11 for MCU power consumption test.

Table 18. Analog input related jumpers

Jumper	Description
JP12	10 KOhm potentiometer RV3 connected to OpAmp2 PA6 when JP12 is closed. **Default setting**: Closed
JP7	Description of JP7 is in *Section 2.7: Audio*

2.17 Comparator

Three I/Os implement a comparator feature as shown in *Figure 8*:

- Comparator non-inverting input PB4; connected to LDR (R157).
- Comparator inverting input PB3; connected to potentiometer (RV3) used as variable threshold input for comparison to luminosity measured on LDR.
- Comparator non-inverting input PB5; connected to potentiometer (RV3) used as analog voltage input for comparison with internal voltage reference (for instance Band gap) in order to test analog Wakeup feature of the MCU.

Figure 8. STM32L152D-EVAL comparator features

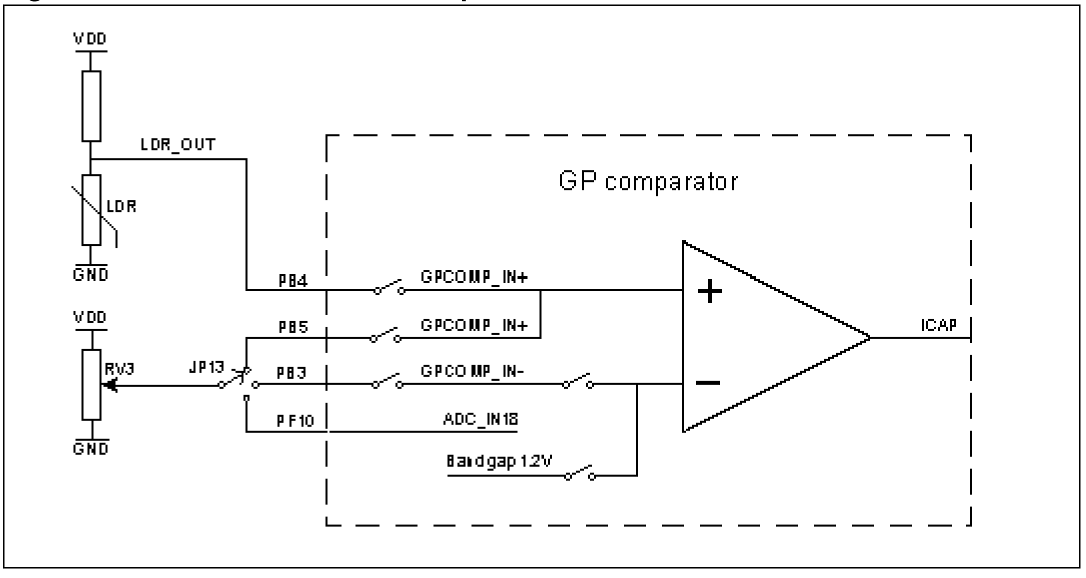
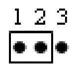
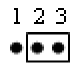
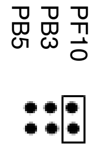
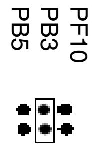
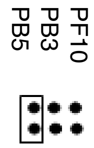


Table 19. Comparator, LDR and potentiometer related jumpers

Jumper	Description	Setting
JP2	PB4 is connected to LDR_OUT when JP2 is set as shown to the right:	
	PB4 is connected to TRST when JP2 is set as shown to the right: (**Default setting**).	
JP13	Potentiometer RV3 is connected to ADC input PF10 used as ADC input when JP13 is set as shown to the right: (**Default setting**).	
	Potentiometer RV3 used as LDR variable threshold input is connected to comparator inverting input GPCOMP_IN- (PB3) when JP13 is set as shown to the right:	
	Potentiometer RV3 is connected to non inverting input GPCOMP_IN+(PB5). The comparator inverting input can be connected to ¼ band gap, ½ band gap, band gap or DAC internally in order to test the possibility to wakeup the MCU when an external voltage reaches a programmable threshold when JP13 is set as shown to the right:	
JP14	PB5 is connected to I2C_SMB, the interrupt output of temperature sensor U24 when JP14 is closed (**Default setting**).	
	PB5 is disconnected from I2C_SMB but remains connected to COM_IN+ when JP14 is open for comparator application.	

The LCD glass module has to be mounted in IO position for comparator usage. Refer to *Section 2.6: LCD glass module* for detail.

2.18 Temperature sensor

Temperature sensor STLM75M2E is connected to the I2C bus of the STM32L152ZDT6 through two transistors to support a wide voltage range from 1.65 V to 3.6 V on the I2C bus.

I2C address of temperature sensor is 0b100100(A0), A0 can be 0 or 1 according to SB9.

Table 20. Temperature sensor related solder bridge

Solder bridge	Description
SB9	I2C address A0 is 0 when SB3 is open. (**Default setting**)
	I2C address A0 is 1 when SB3 is closed.

The LCD glass module has to be mounted on IO position for temperature sensor usage. Refer to *Section 2.6: LCD glass module* for detail.

Note: Temperature result measured from STLM75M2E would be a little higher than ambient temperature due to board heat.

2.19 Display and input devices

The display devices are 4 general purpose color LED's (LD 1,2,3,4) and a 240x320 TFT color LCD connected to bank3 of the STM32L152ZDT6 FSMC interface port. The LCD glass module must be mounted on IO position for color LCD usage. Refer to *Section 2.6: LCD glass module* for detail.

Input devices are the 4-direction joystick (U23) with selection key and wakeup button (B2).

Three LCD references using different controllers can be mounted on LCD board MB895, as shown in *Table 21*. The driver provided in the library is able to identify which LCD is used by reading the controller ID, and then to adapt communication according to each controller specificity. The LCD references and corresponding controllers used are summarized below:

Table 21. LCD references

LCD reference	Controller	Controller manufacturer
AM-240320LDTNQW-02H	SPFD5408B	Orise Technology
AM-240320LDTNQW-05H	RM68050	Raydium
AM240320LGTNQW-01H	HX-8347D	Himax

Table 22. LCD modules

Pin	Description	Pin connection
1	CS	CS of Bank3 of FSMC
2	RS	FSMC_A0
3	WR/SCL	FSMC_NWE
4	RD	FSMC_NOE
5	RESET	RESET#
6	PD1	FSMC_D0
7	PD2	FSMC_D1
8	PD3	FSMC_D2
9	PD4	FSMC_D3
10	PD5	FSMC_D4
11	PD6	FSMC_D5
12	PD7	FSMC_D6
13	PD8	FSMC_D7
14	PD10	FSMC_D8
15	PD11	FSMC_D9
16	PD12	FSMC_D10
17	PD13	FSMC_D11

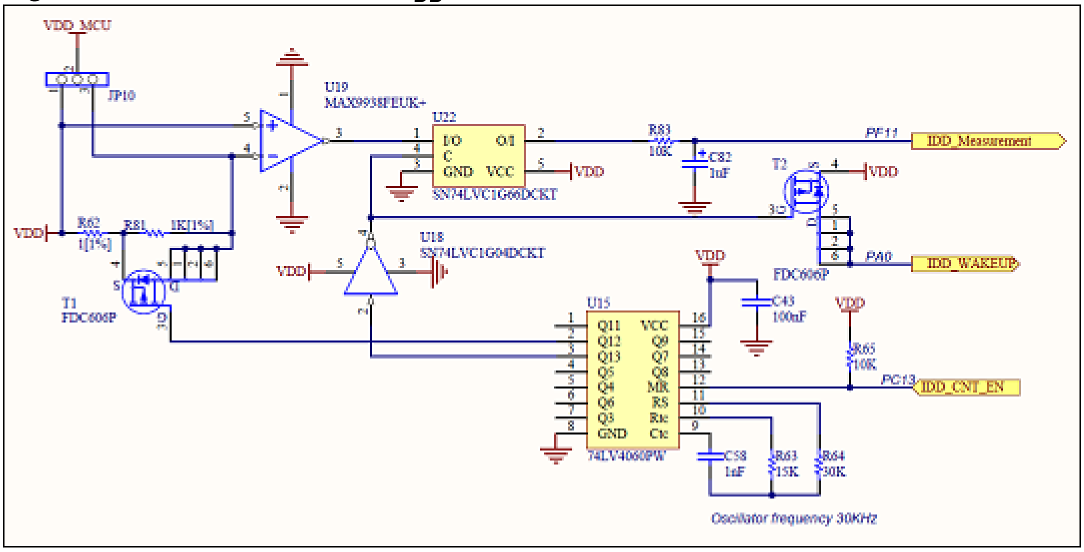
Table 22. LCD modules (continued)

Pin	Description	Pin connection
18	PD14	FSMC_D12
19	PD15	FSMC_D13
20	PD16	FSMC_D14
21	PD17	FSMC_D15
22	BL_GND	GND
23	BL_control	5V
24	VDD	3.3V
25	VCI	3.3V
26	GND	GND
27	GND	GND
28	BL_VDD	5V
29	SDO	-
30	SDI	GND

2.20 I_{DD} measurement

The built-in I_{DD} measurement circuit implemented allows the consumption measurement of the STM32L152ZDT6 while the MCU is in Run or Low power saving modes.
For I_{DD} measurement the circuit below is implemented on the STM32L152D-EVAL.

Figure 9. STM32L152D-EVAL I_{DD} measurement circuit



2.20.1 Run mode

In Run mode, I_{DD} current is measured using operational amplifier MAX9938FEUK+ (U19) connected to the 1 Ohm shunt resistor (R62). In this case IDD_CNT_EN remains high

during measurement, so R81 remains in short-circuit during measurement because of transistor T1 which remains ON permanently. JP10 must be connected between pins 2 & 3.

2.20.2 Low power mode

In Low power modes (Stop or Standby), the operational amplifier MAX9938FEUK+ (U19) is connected to the 1 KOhm shunt resistor (R81), controlled by the analog switch T1. In this case the counter 74HC4060 (U15) enabled by IDD_CNT_EN manages the measurement timing according to *Figure 10*.

The principle used to measure a current when the STM32L is in Low power mode is:

1. Configure ADC to measure voltage on the IDD_Measurement pin (PF11).
2. Configure PA0 to serve as wakeup pin.
3. Enter Low power mode after setting IDD_CNT_EN (PC13) signal low.
4. IDD_WAKEUP rising edge wakes up the MCU after around 300 ms.
5. Start ADC conversion as soon as possible after wakeup in order to measure the voltage corresponding to Low power mode on capacitor C82.
6. Reset the counter by programming IDD_CNT_EN high (in less than 70 ms after the wakeup) to avoid the R81 (1 KOhm) resistor being connected later in Run mode.

In Low power modes, the 1 K resistor is connected when T1 goes off after entering Low power mode. Q12 output of the counter allows connection of the 1 K resistor when the current I_{DD} becomes very low.

Figure 10. STM32L152D-EVAL I_{DD} Low power modes measurement timing diagram

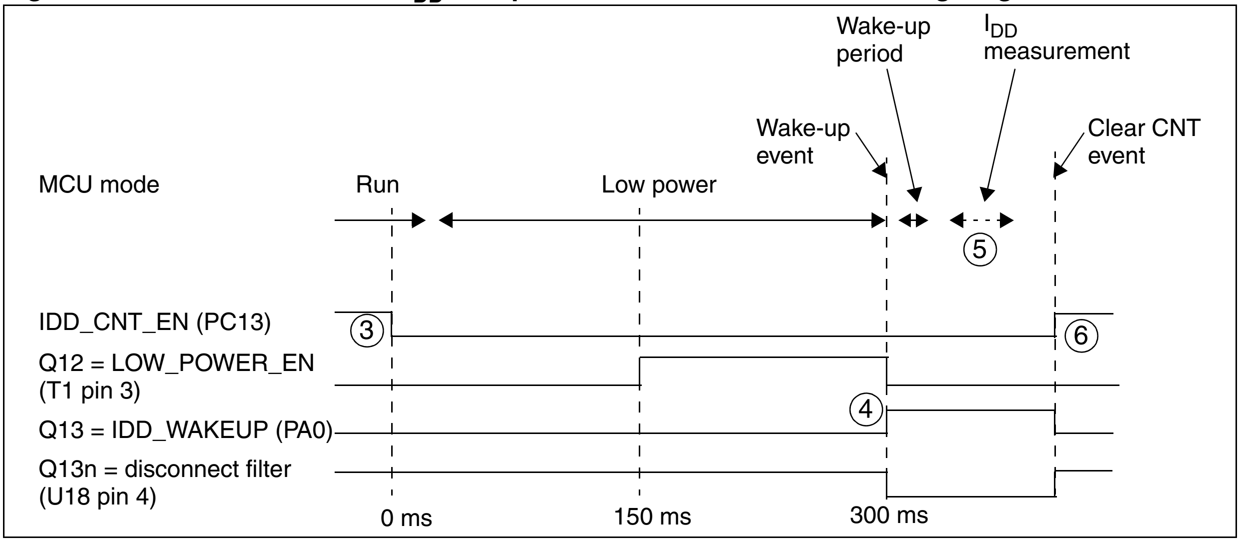


Figure 10 shows how the counter and T1 ensure that, 150 ms after IDD_CNT_EN falling edge, the shunt resistor R81 is connected between VDD_MCU and the power supply in order to reduce the measurement range to 30 uA full scale when VDD = 1.8 V.
Then after another 150 ms for current stabilization, R81 is shorted, the I_{DD} measurement is stored in C82, and the MCU is woken up. After wakeup the MCU can measure the I_{DD} current corresponding to the Low power mode stored in C82.

2.20.3 Ibias current measurement procedure

In Low power mode the bias current of operational amplifier input (U19 pin 4) is not negligible compared to I_{DD} current (typical Ibias is ~240 nA). To obtain a reliable MCU I_{DD} measurement it is possible to subtract the bias current from the I_{DD} low power measurement since this current is not sinked by the MCU. The procedure for accurate I_{DD} measurement is:

1. Set jumper JP10 on pin 1 and pin 2.
2. Follow the Low power mode procedure to measure I1 = I bias.
3. Remove jumper JP10 from pins 1 and 2 and place it on pins 2 and 3.
4. Follow the Low power mode procedure to measure I2 = I_{DD} + I bias.
5. Calculate actual I_{DD}: I_{DD} = I2 - I1.

If JP10 jumper is in pins 2-3: STM32L is powered through I_{DD} measurement circuit (default). If JP10 jumper is in pins1-2: STM32L is powered directly by +3V3, I_{DD} measurement circuit is bypassed. Refer to *Section 2.2: Power supply* for detail.

Note: 1 When jumper JP10 is removed the current consumption of the STM32L can be measured by connecting an ammeter between jumper JP10, pins 1 and 2.

2 RDS (on) typical value of analog switch T1= 50 MOhm, so to improve measurement accuracy it is recommended to take into account the RDS in series with R62 (1 Ohm) in the I_{DD} Run mode current calculation.

3 To avoid current injection from MCU to components on the board during I_{DD} measurement it is strongly recommended to keep VDD_MCU ≤ 3.3 V. Some components on the board are powered by 3.3 V (for instance the ST-LINK) so if VDD_MCU is higher than 3.3 V a current can be in injected on signals like T_NRST (PB0 of U21) which disturbs the measurement in low power mode.

3 Connectors

3.1 RS-232 connector CN1

Figure 11. RS-232 connector (viewed from front)

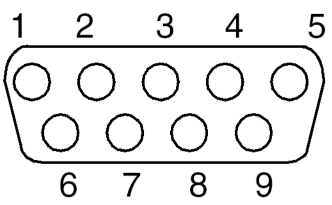


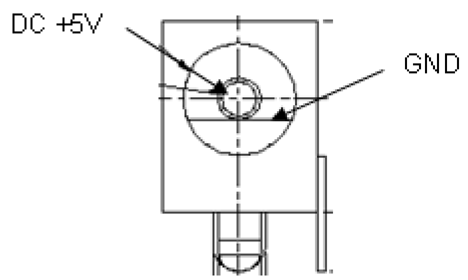
Table 23. RS-232 connector CN1 with HW flow control and ISP support

Pin	Description	Pin	Description
1	NC	6	Bootloader_BOOT0
2	RS-232_RX (PB11)	7	NC
3	RS-232_TX (PB10)	8	Bootloader_RESET
4	NC	9	NC
5	GND		

3.2 Power connector CN2

The STM32L152D-EVAL evaluation board can be powered from a DC 5 V power supply via the external power supply jack (CN2) shown in *Figure 12*. The central pin of CN2 must be positive.

Figure 12. Power supply connector CN2 (viewed from front)



3.3 TFT LCD connector CN4

A TFT color LCD board (MB895) is mounted on CN4.

3.4 Daughterboard extension connector CN5 and CN10

Two 42-pin male headers CN5 and CN10 can connect the daughterboard (or standard wrapping board) to the STM32L152D-EVAL evaluation board. All GPIOs are available on them and the LCD glass connectors (CN6, CN7).

The space between these two connectors and positions of POWER, GND and RESET pins are defined as a standard which allows common daughterboards to be developed for several evaluation boards. The standard width between CN5 pin1 and CN10 pin1 is 2700 mils (68.58 mm). This standard has been implemented on the majority of evaluation boards.

Each pin on CN5 and CN10 can be used by a daughterboard after disconnecting it from the corresponding function block on the STM32L152D-EVAL evaluation board. Refer to *Table 24* and *Table 25* for detail.

Table 24. Daughterboard extension connector CN5

Pin	Description	Alternative function	How to disconnect with function block on STM32L152D-EVAL board
1	GND	-	-
3	PF5	FSMC_A5	-
5	PF3	FSMC_A3	-
7	PF1	FSMC_A1	-
9	PE6	Tamper / Key / U5V_DET	Remove R150
11	PC14	32K OSC	Remove R85 and close SB8
13	PE5	FSMC_A21 / TRACED2	-
15	PC15	32K OSC	Remove R84 and close SB7
17	PA4	CON_ADC4 -DAC1 / Audio_DAC_OUT	JP7 open
19	GND	-	-
21	PB2	BOOT1	Remove R89
23	PF12	FSMC_A6	-
25	PF14	FSMC_A8	-
27	PG0	FSMC_A10	-
29	PE7	FSMC_D4	-
31	VLCD	-	-
33	PE9	FSMC_D6	-
35	PE11	FSMC_D8	-
37	PE13	FSMC_D10	-
39	GND	-	-
41	PG2	FSMC_A12	-
2	-	-	-

Table 24. Daughterboard extension connector CN5 (continued)

Pin	Description	Alternative function	How to disconnect with function block on STM32L152D-EVAL board
4	PF4	FSMC_A4	-
6	PF2	FSMC_A2	-
8	PF0	FSMC_A0	-
10	GND	-	-
12	PE4	FSMC_A20 / TRACED1	Remove R147
14	PF10	POTENTIOMETER	JP13 pin5,6 open
16	PA0	IDD_WAKEUP / KEY_TAMPER2 /WKUP1	Remove R118
18	PA5	E2P_SCK	-
20	-	-	-
22	PF11	IDD_measurement	Remove R83,C82
24	PF13	FSMC_A7	-
26	PF15	FSMC_A9	-
28	PG1	FSMC_A11	-
30	GND	-	-
32	PE8	FSMC_D5	-
34	PE10	FSMC_D7	-
36	PE12	FSMC_D9	-
38	PE14	FSMC_D11 / E2P_ MISO	Remove R90
40	PE15	FSMC_D12 / E2P_ MOSI	Remove R120
42	+3.3	-	If use 3.3 V power, keep R24 mounting

Table 25. Daughterboard extension connector CN10

Pin	Description	Alternative function	How to disconnect with function block on STM32L152D-EVAL board
1	GND	-	-
3	PB7	C_Shield_CT_6_4	Remove R101 and close SB11
5	PG15	LED4	Remove R60
7	PG13	JOYSTICK_SELECT	Remove R105
9	PC13	IDD_CNT_EN	-
11	RESET#	-	-
13	PG10	CS_RAM_EBAR2	Remove R40
15	PD7	LED2	Remove R71
17	PD5	FSMC_WEN	-
19	D5V	-	-

Table 25. Daughterboard extension connector CN10 (continued)

Pin	Description	Alternative function	How to disconnect with function block on STM32L152D-EVAL board
21	PD1	FSMC_D3	-
23	PH0	OSC_IN	Remove X1 from socket and close SB2
25	PA14	JTCK/SWCLK	-
27	PH2	FSMC_A22	-
29	PA12	USB_DP	Remove R136
31	PA11	USB_DM	Remove R149
33	PG7	JOYSTICK_RIGHT	Remove R117
35	PF6	SLIDER_CT_11_1	Remove R77 and close SB6
37	PF8	SLIDER_CT_11_3	Remove R69 and close SB4
39	GND	-	-
41	PG4	FSMC_A14	-
2	-	-	-
4	PB6	Shield_CT_6_3	Remove R92 and close SB10
6	PG14	LED3	Remove R67
8	PG12	LCD_EBAR3	-
10	GND	-	-
12	PG11	JOYSTICK_UP	Remove R119
14	PG9	CS_NOR_EBAR1	Remove R31
16	PD6	FSMC_WAITN	-
18	PD4	FSMC_OEN	-
20	PD3	LED1	Remove R74
22	PD0	FSMC_D2	-
24	VDD	-	-
26	PH1	OSC_OUT	Remove X1 from socket & close SB1
28	PA13	JTMS/SWDAT	-
30	GND	-	-
32	PG8	JOYSTICK_DOWN	Remove R110
34	PG6	JOYSTICK_LEFT	Remove R104
36	PF7	SLIDER_CT_11_2	Remove R73 and close SB5
38	PF9	SLIDER_CT_11_4	Remove C54 and close SB3
40	PG5	FSMC_A15	-
42	PG3	FSMC_A13	-

3.5 LCD glass daughterboard connectors CN6 and CN7

Two 48-pin male headers CN6 and CN7 connect the LCD glass daughterboard (MB979). GPIOs which act as LCD glass signals and are not on CN5 and CN10 are available on these two connectors. The space between these two connectors and the position of every LCD glass signal is defined as a standard which allows development of common daughterboards for several evaluation boards. The standard width between the CN7 pin1 and CN6 pin1 is 700 mils (17.78 mm).

GPIO signals on these two connectors can be tested on odd pins when the LCD glass board is absent. Signal assignments are detailed in *Table 26*.

Note: If CN6 and CN7 are used as GPIO extension connector on a common daughterboard, do not connect odd pins and even pins directly onto the daughterboard, and leave Trace connector (CN11), JTAG connector (CN16) and JP2 open.

Table 26. LCD glass daughterboard connectors CN6 and CN7

CN7		CN6	
Odd pin	**GPIO signal**	**Odd pin**	**GPIO signal**
1	PA9	1	PD2
3	PA8	3	PC12
5	PA10	5	PC11
7	PB9	7	PC10
9	PB11	9	PC3
11	PB10	11	PC4
13	PB5	13	PC5
15	PB14	15	PC6
17	PB13	17	PC7
19	PB12	19	PC8
21	PA15	21	PC9
23	PB8	23	PD8
25	PB15	25	PD9
27	PC2	27	PD10
29	PC1	29	PD11
31	PC0	31	PD12
33	PA3	33	PD13
35	PA2	35	PD14
37	PB0	37	PD15
39	PA7	39	PE0
41	PA6	41	PE1
43	PB4	43	PE2
45	PB3	45	PE3
47	PB1	47	PA1

3.6 ST-LINK/V2 programming connector CN9

Connector CN9 is used only for embedded ST-LINK/V2 programming during board manufacture. It is not populated by default and is not for end-user use.

3.7 ST-LINK/V2 USB type B connector CN14

The USB connector CN14 is used to connect the embedded ST-LINK/V2 to a PC for debugging the board.

Figure 13. USB type B connector CN14 (viewed from front)

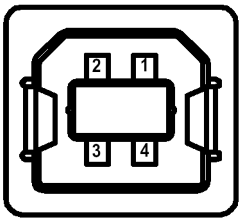


Table 27. USB type B connector CN14

Pin	Description	Pin	Description
1	VBUS (power)	4	GND
2	DM	5,6	Shield
3	DP		

3.8 JTAG connector CN16

Figure 14. JTAG debugging connector CN16 (viewed from above PCB)

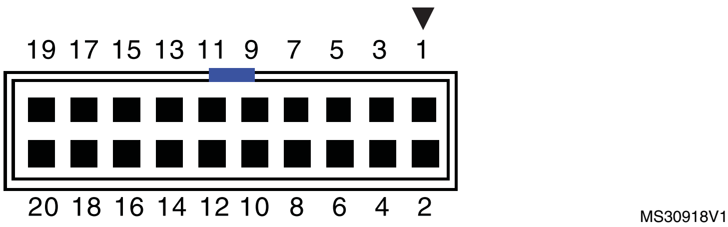


Table 28. JTAG debugging connector CN16

Pin	Description	Pin	Description
1	VDD power	2	VDD power
3	PB4	4	GND
5	PA15	6	GND
7	PA13	8	GND
9	PA14	10	GND

Table 28. JTAG debugging connector CN16 (continued)

Pin	Description	Pin	Description
11	RTCK	12	GND
13	PB3	14	GND
15	RESET#	16	GND
17	DBGRQ	18	GND
19	DBGACK	20	GND

3.9 Trace debugging connector CN11

Figure 15. Trace debugging connector CN11 (viewed from above PCB)

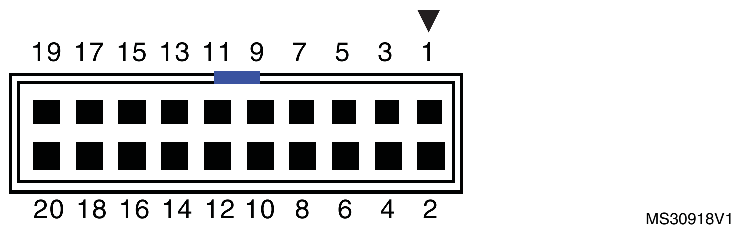


Table 29. Trace debugging connector CN11

Pin	Description	Pin	Description
1	VDD power	2	TMS/PA13
3	GND	4	TCK/PA14
5	GND	6	TDO/PB3
7	KEY	8	TDI/PA15
9	GND	10	RESET#
11	GND	12	TraceCLK/PE2
13	GND	14	TraceD0/PE3 or SWO/PB3
15	GND	16	TraceD1/PE4 or nTRST/PB4
17	GND	18	TraceD2/PE5
19	GND	20	TraceD3/PE6

3.10 Audio jack CN13

A 3.5 mm stereo audio jack CN13 connected to audio DAC is available on the STM32L152D-EVAL board.

3.11 MicroSD connector CN3

Figure 16. MicroSD connector CN3 (viewed from above PCB)

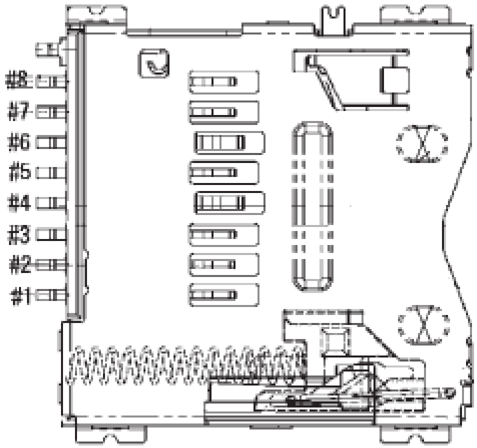


Table 30. MicroSD connector CN3

Pin	Description	Pin	Description
1	SDIO_D2(PC10)	6	Vss/GND
2	SDIO_D3(PC11)	7	SDIO_D0(PC8)
3	SDIO_CMD(PD2)	8	SDIO_D1(PC9)
4	VDD	9	GND
5	SDIO_CLK(PC12)	10	MicroSDcard_detect (PC7)

3.12 Analog input-output 2-pin connector CN8

Figure 17. Analog input-output connector CN8 (viewed from top)

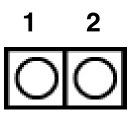


Table 31. Analog input-output connector CN8

Pin	Description	Pin	Description
1	GND	2	Analog input-output PA4

3.13 User USB type B connector CN15

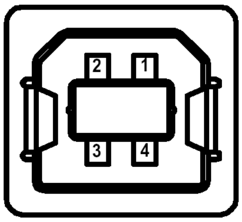


Figure 18. USB type B connector CN15 (viewed from front)

Table 32. USB type B connector CN15

Pin	Description	Pin	Description
1	VBUS (power)	4	GND
2	DM	5,6	Shield
3	DP		

3.14 RF EEPROM daughterboard connector CN12

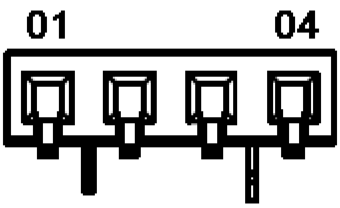


Figure 19. RF EEPROM daughterboard connector CN12 (viewed from front)

Table 33. USB type B connector CN15

Pin	Description	Pin	Description
1	SDA(PB9)	3	VDD
2	SCL(PB8)	4	GND

4 Schematics

Figure 20. STM32L152D-EVAL

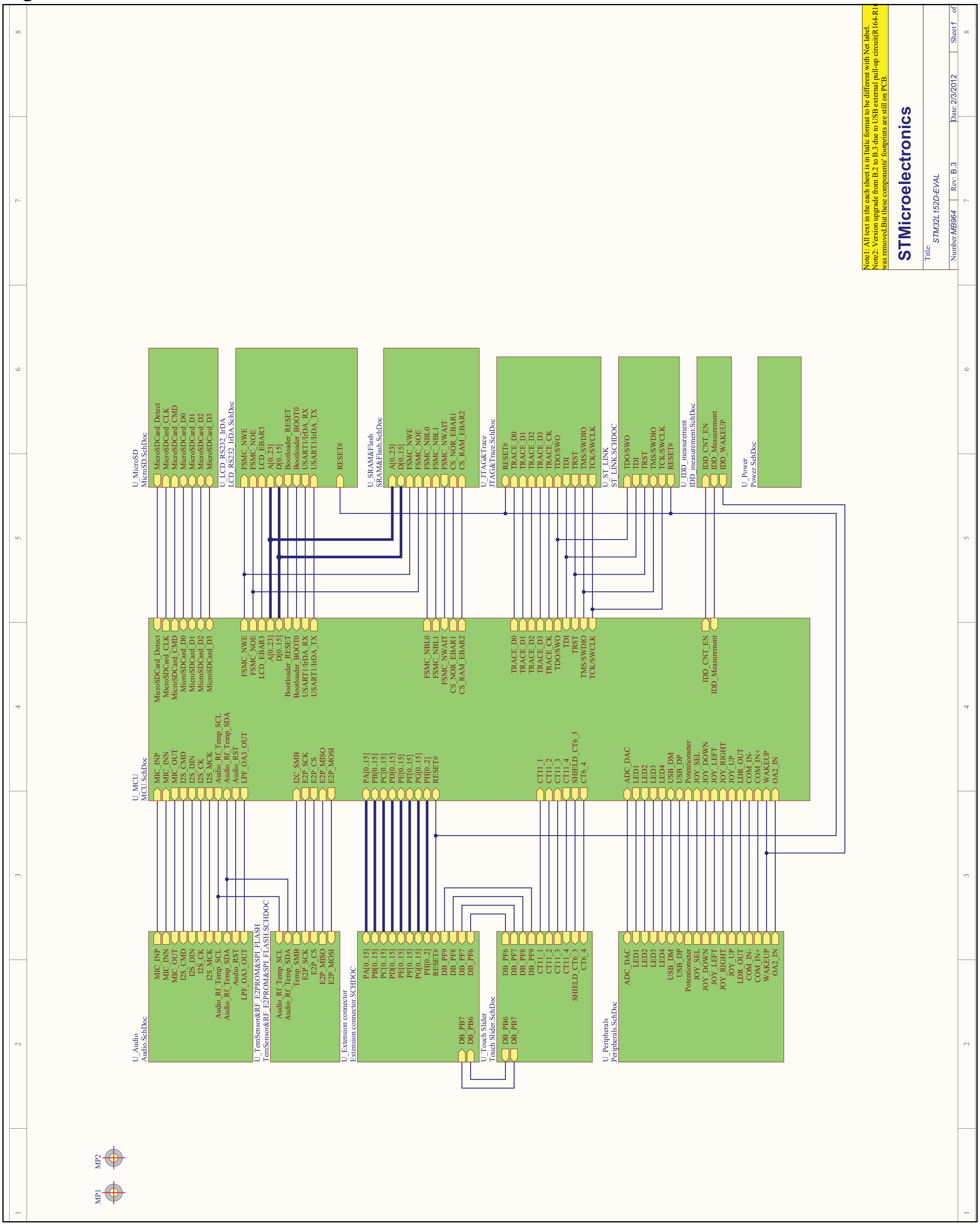


Figure 21. Audio

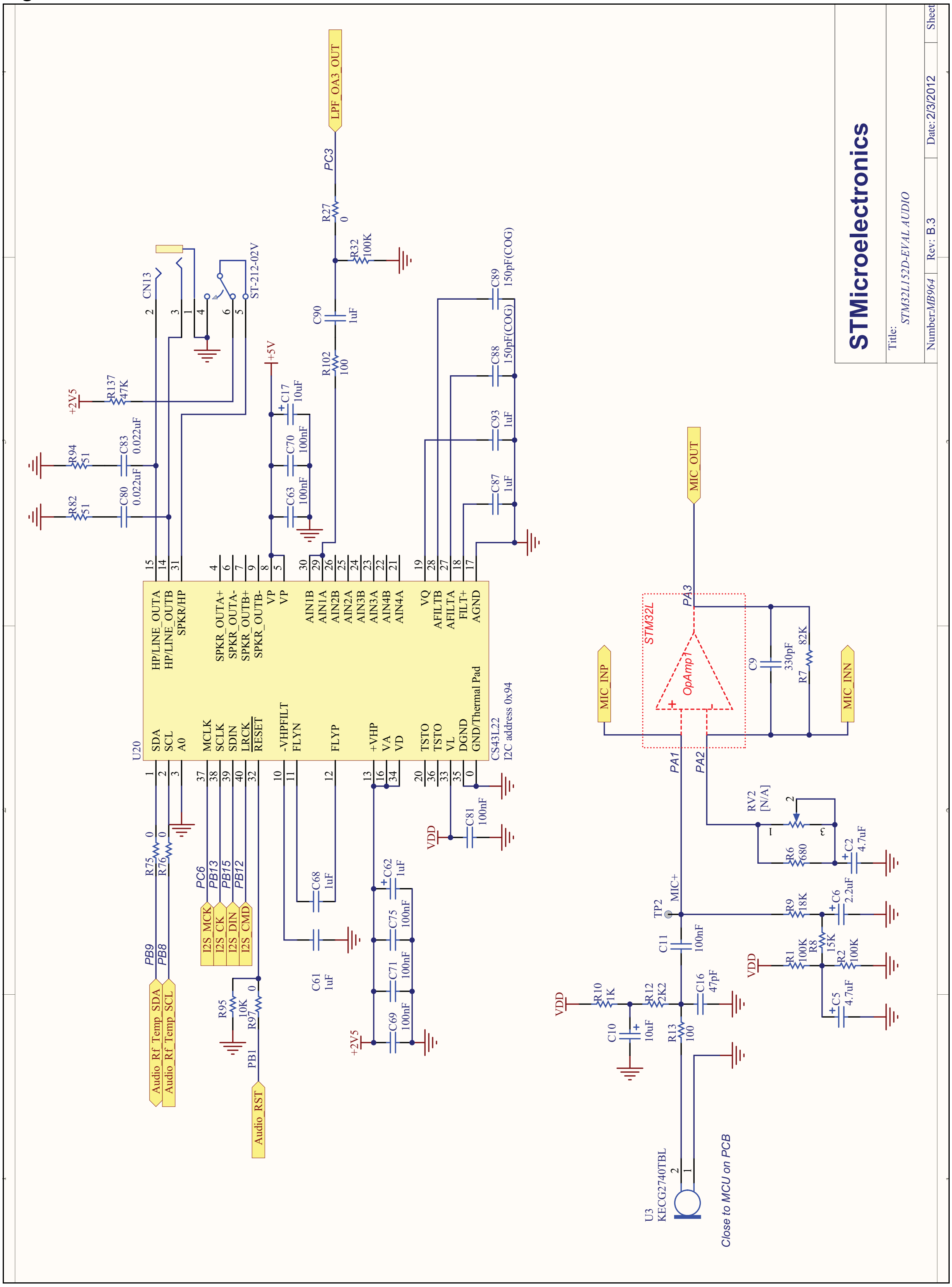


Figure 22. Extension connector

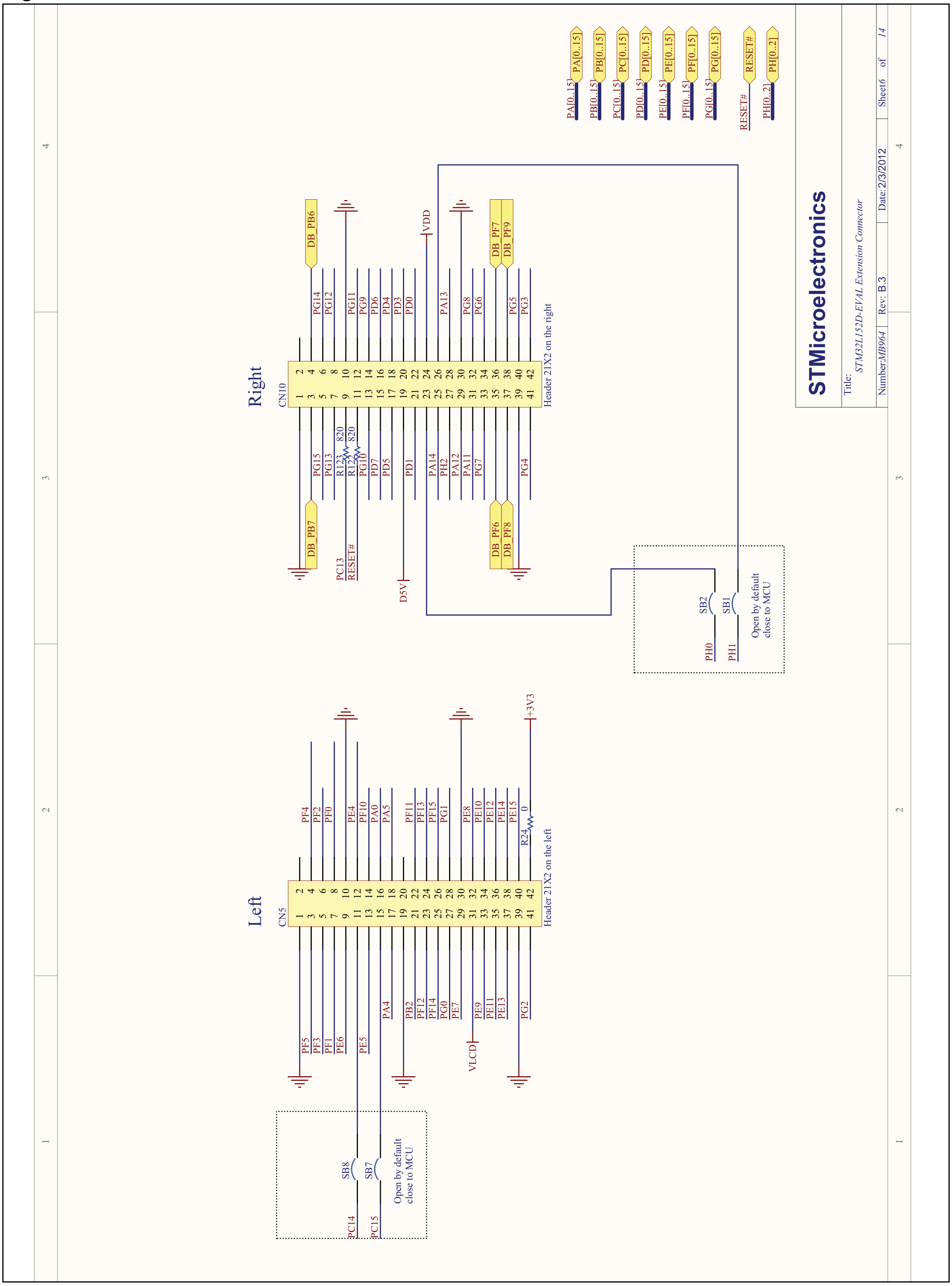


Figure 23. I_{DD} measurement

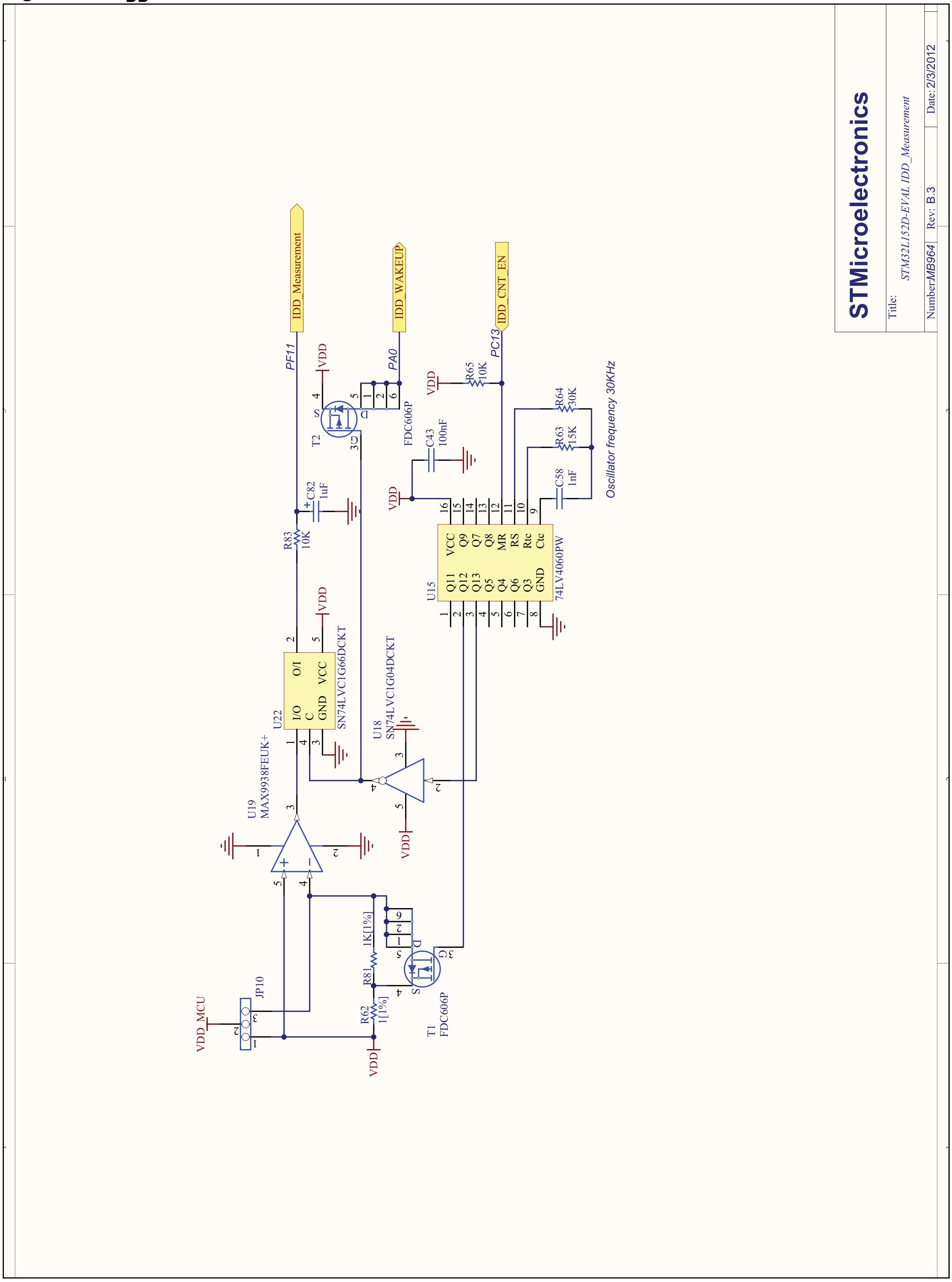


Figure 24. JTAG and Trace

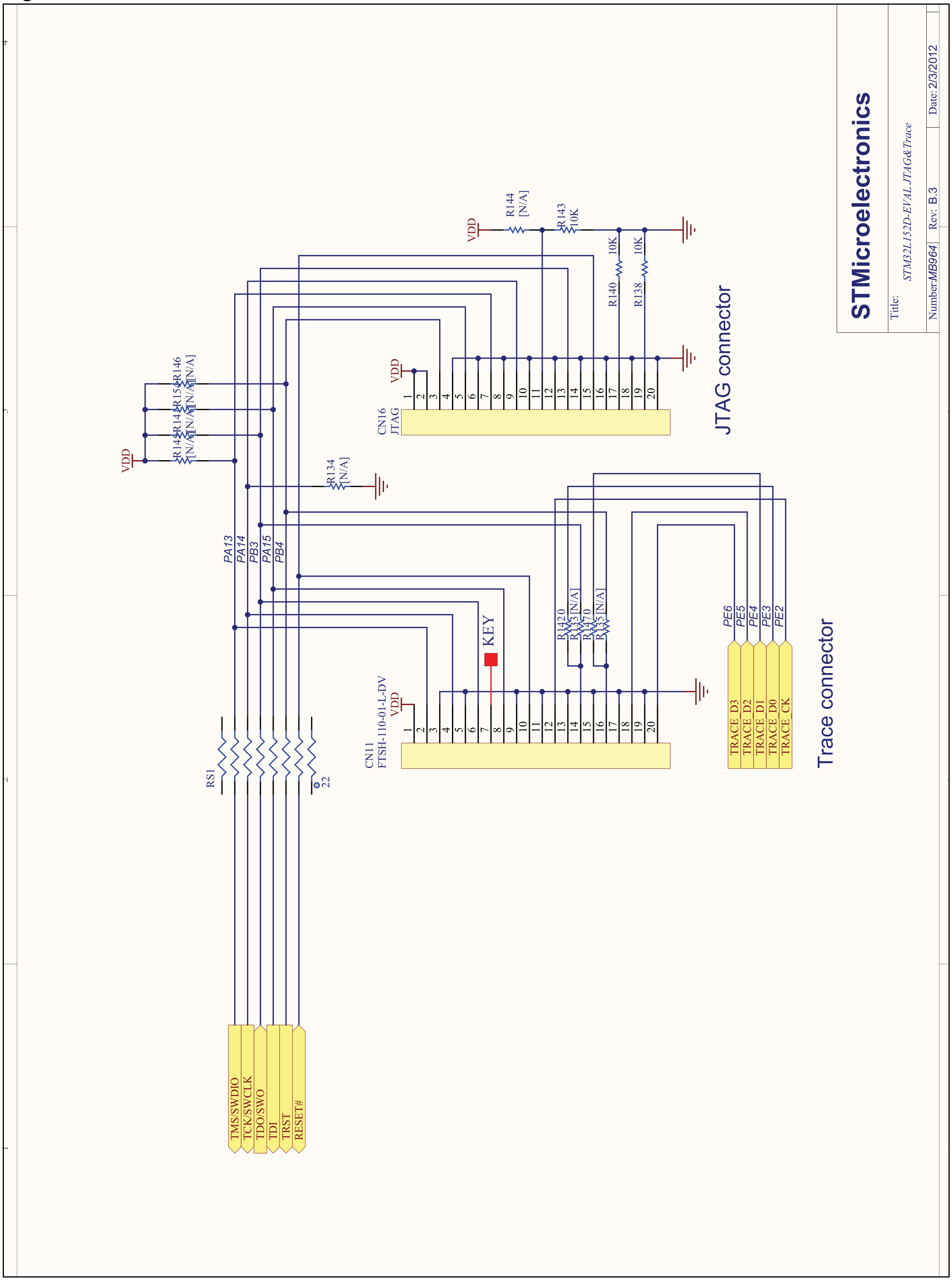


Figure 25. RS-232 and LCD

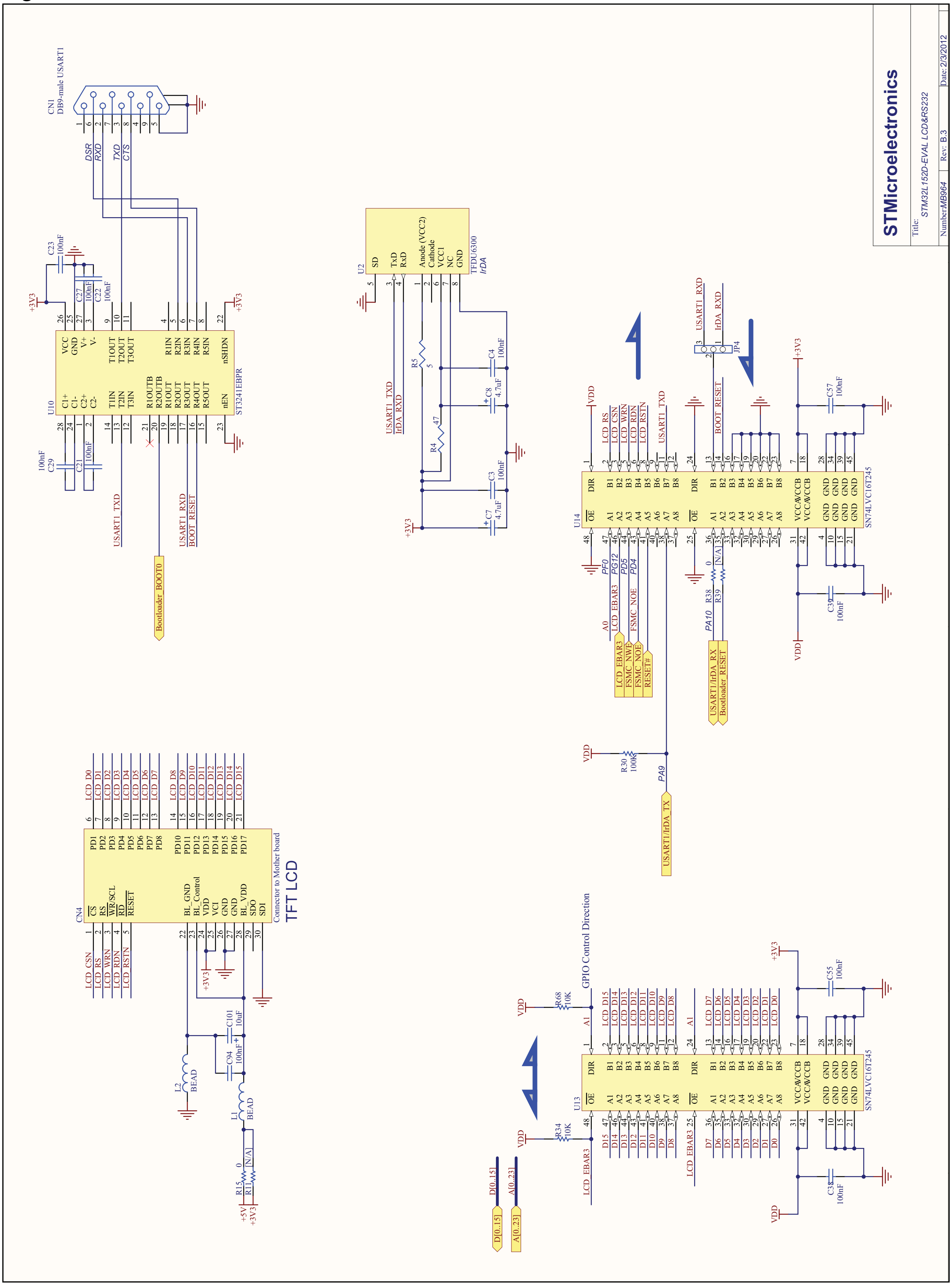


Figure 26. MCU

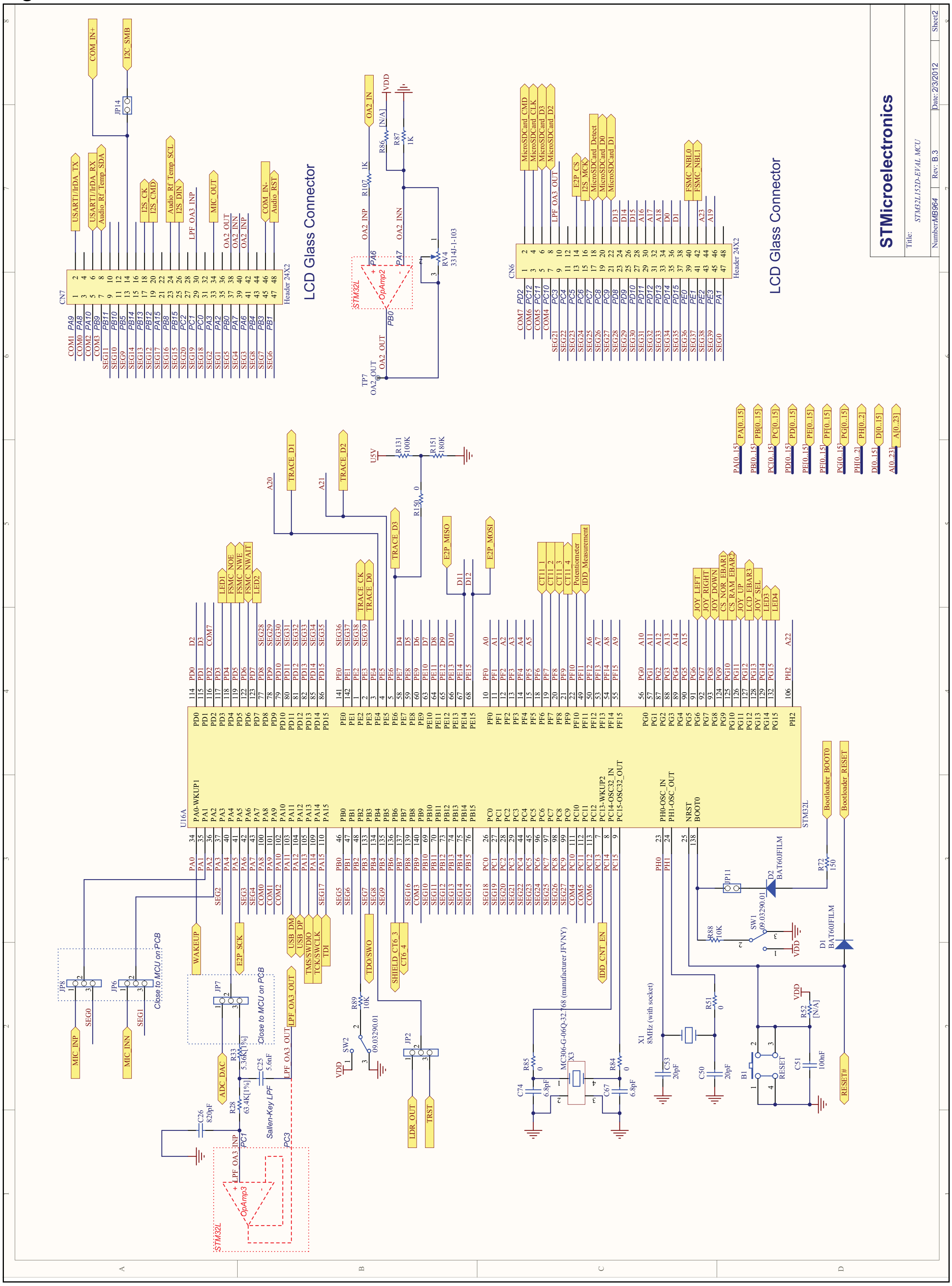


Figure 27. MicroSD Card

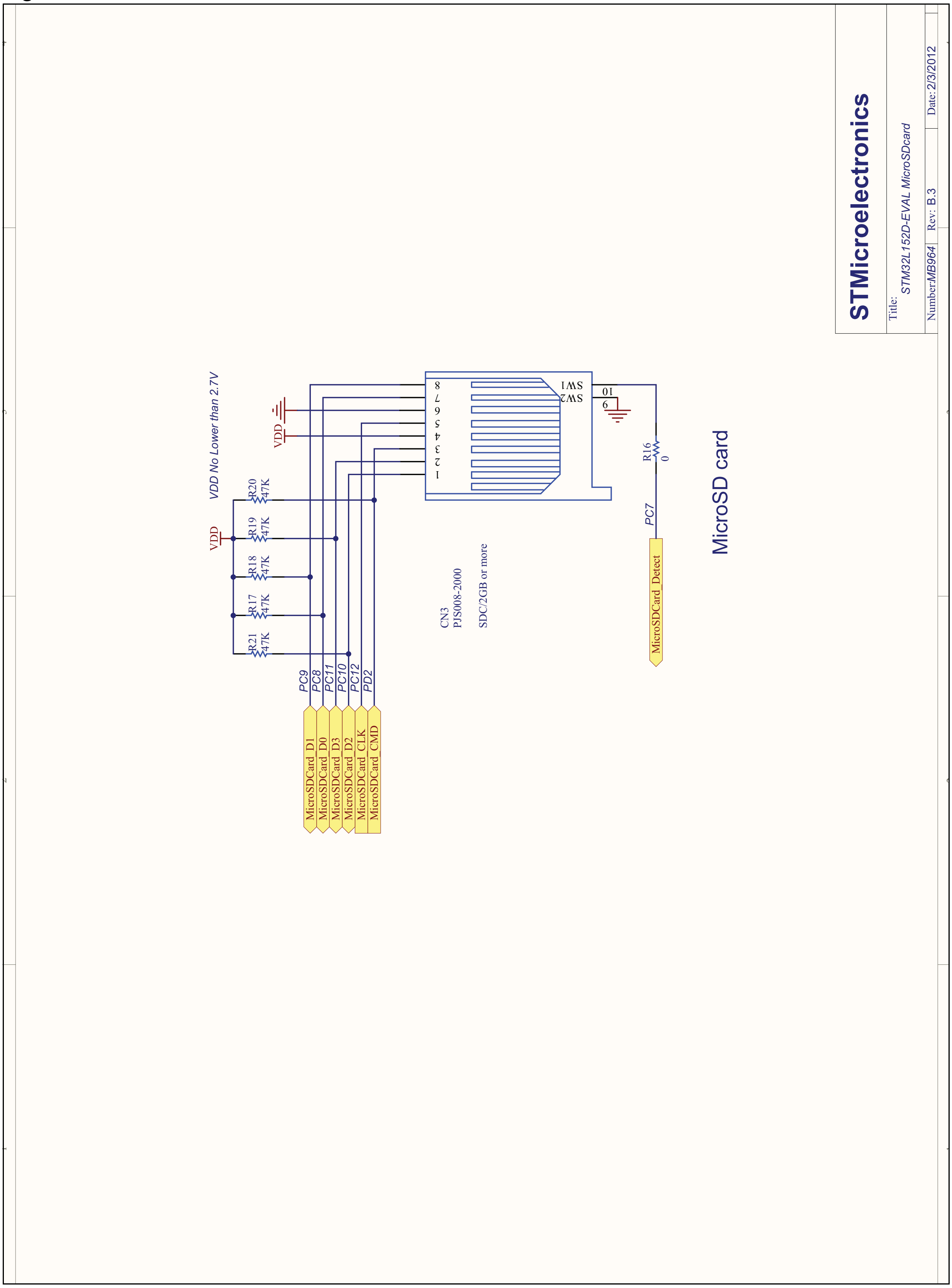


Figure 28. Peripherals

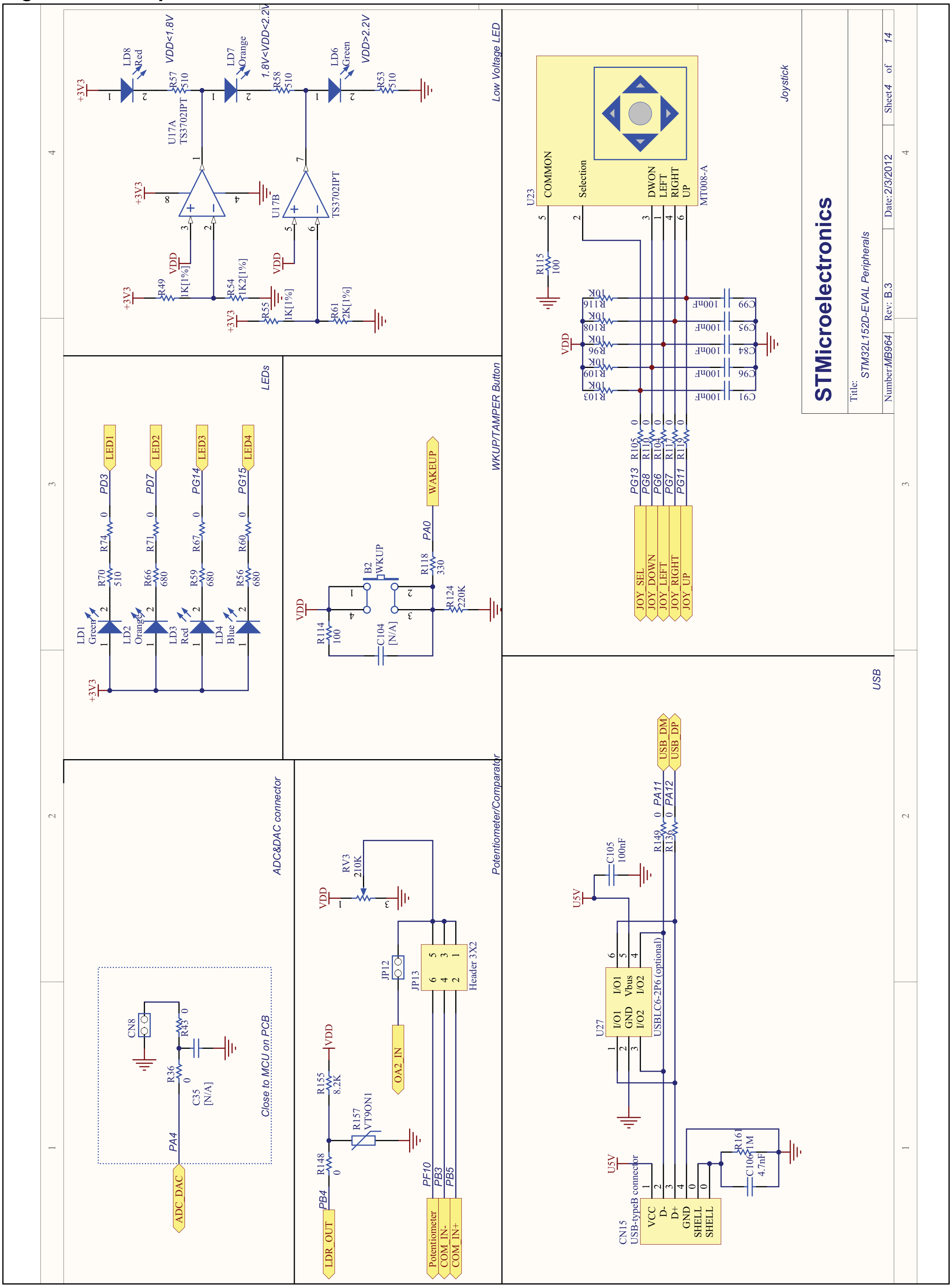


Figure 29. Power

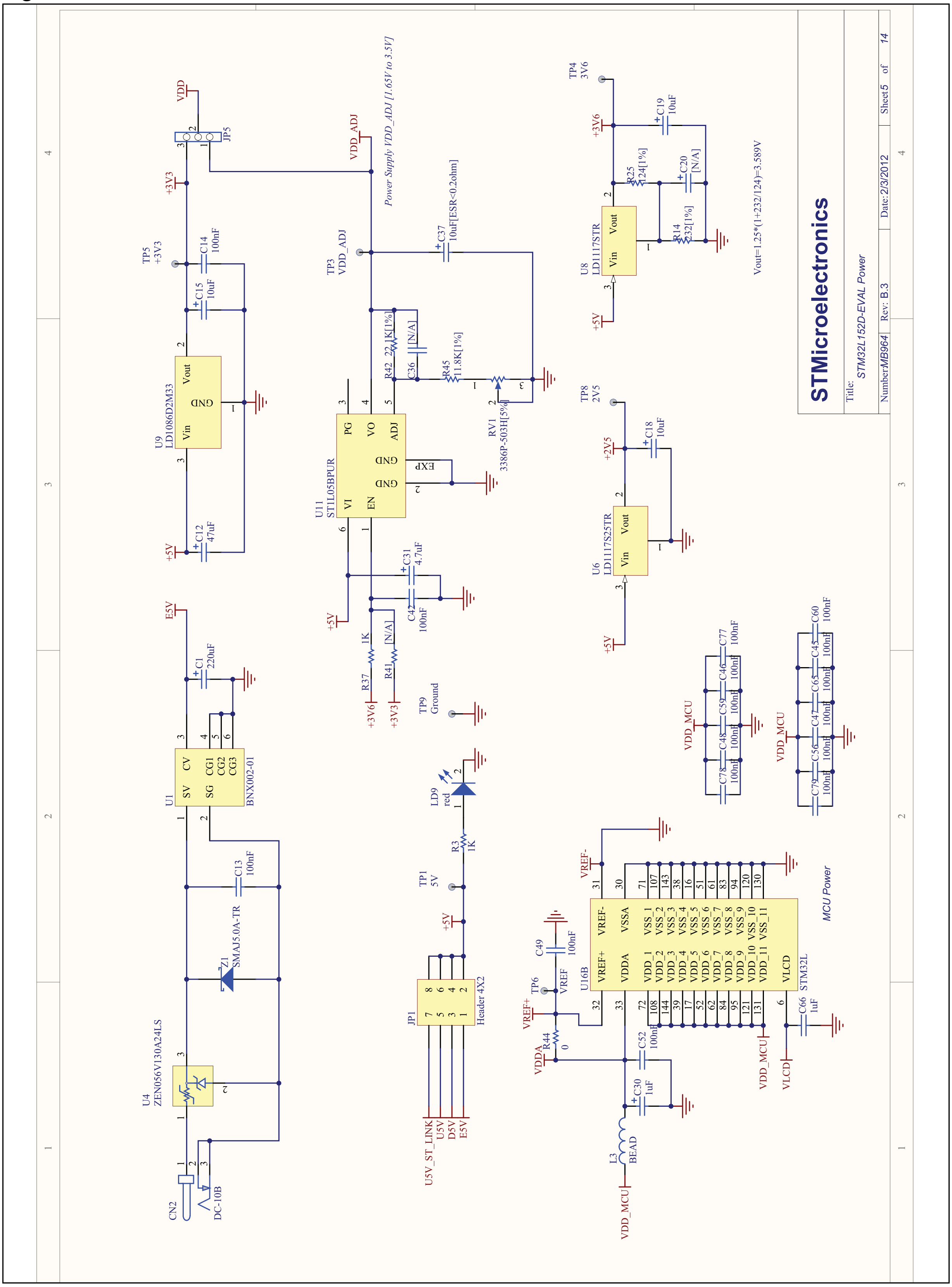


Figure 30. SRAM Flash

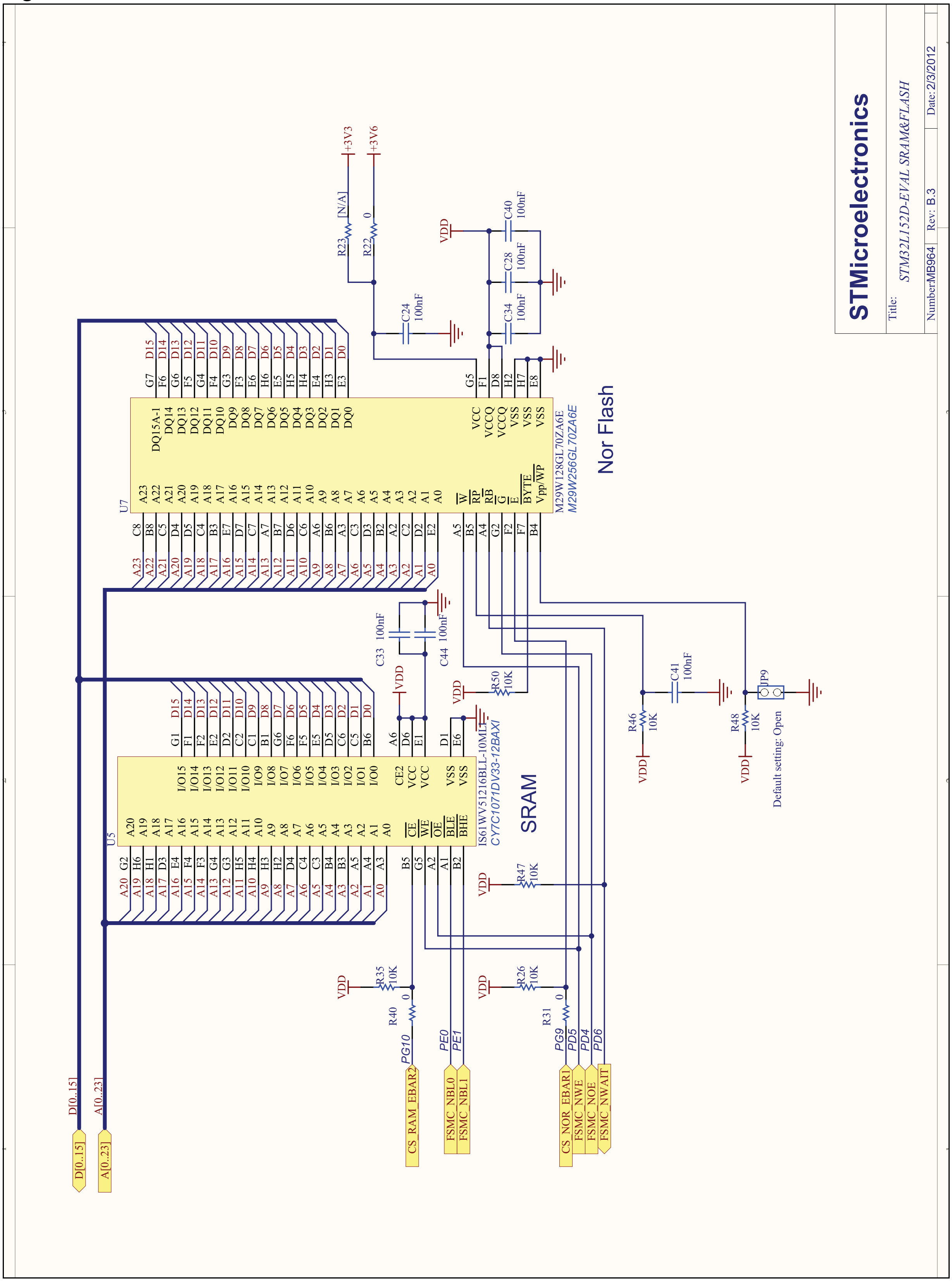


Figure 31. ST_LINK

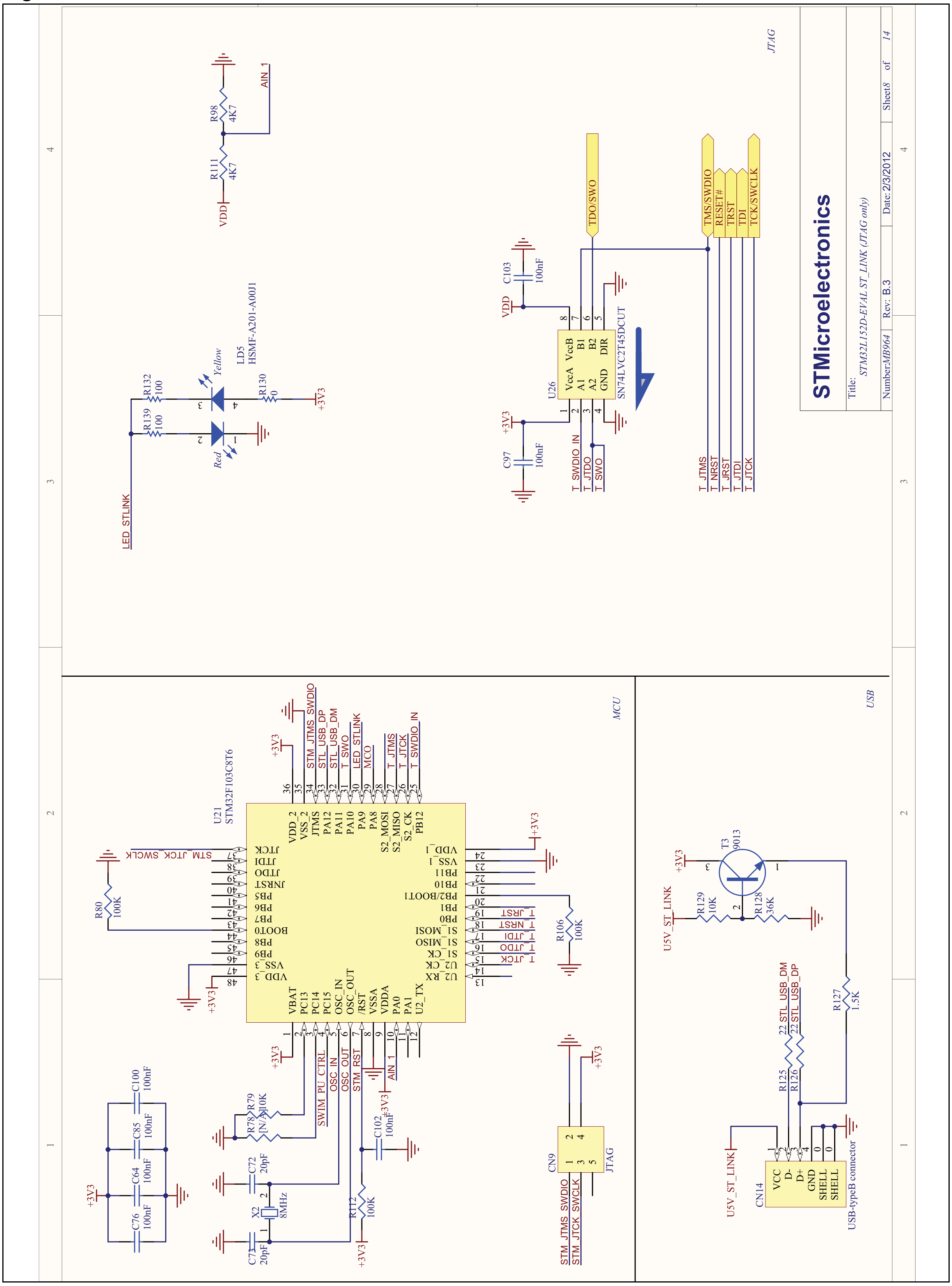


Figure 32. EEPROM and temperature sensor

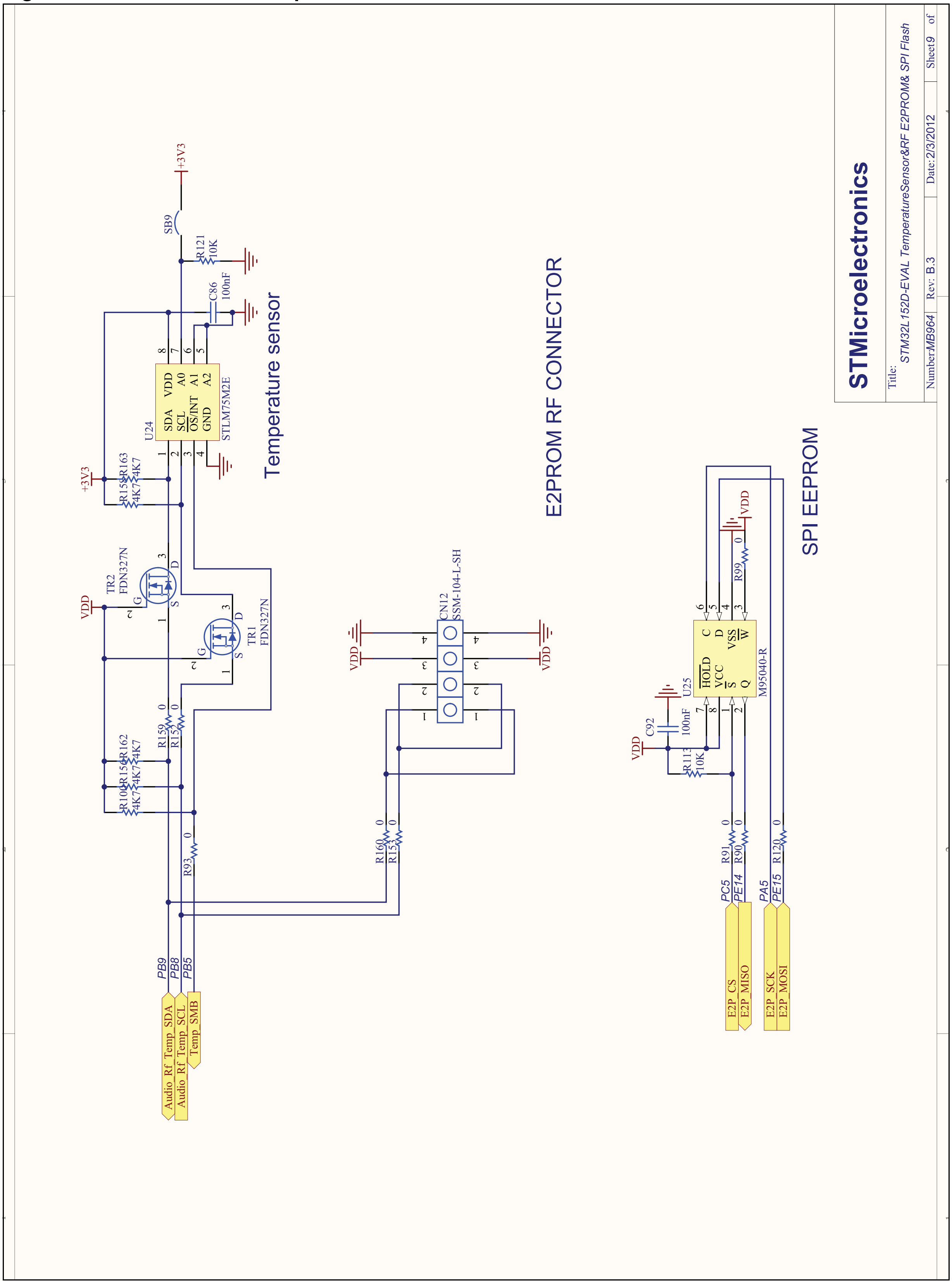


Figure 33. Touch slider

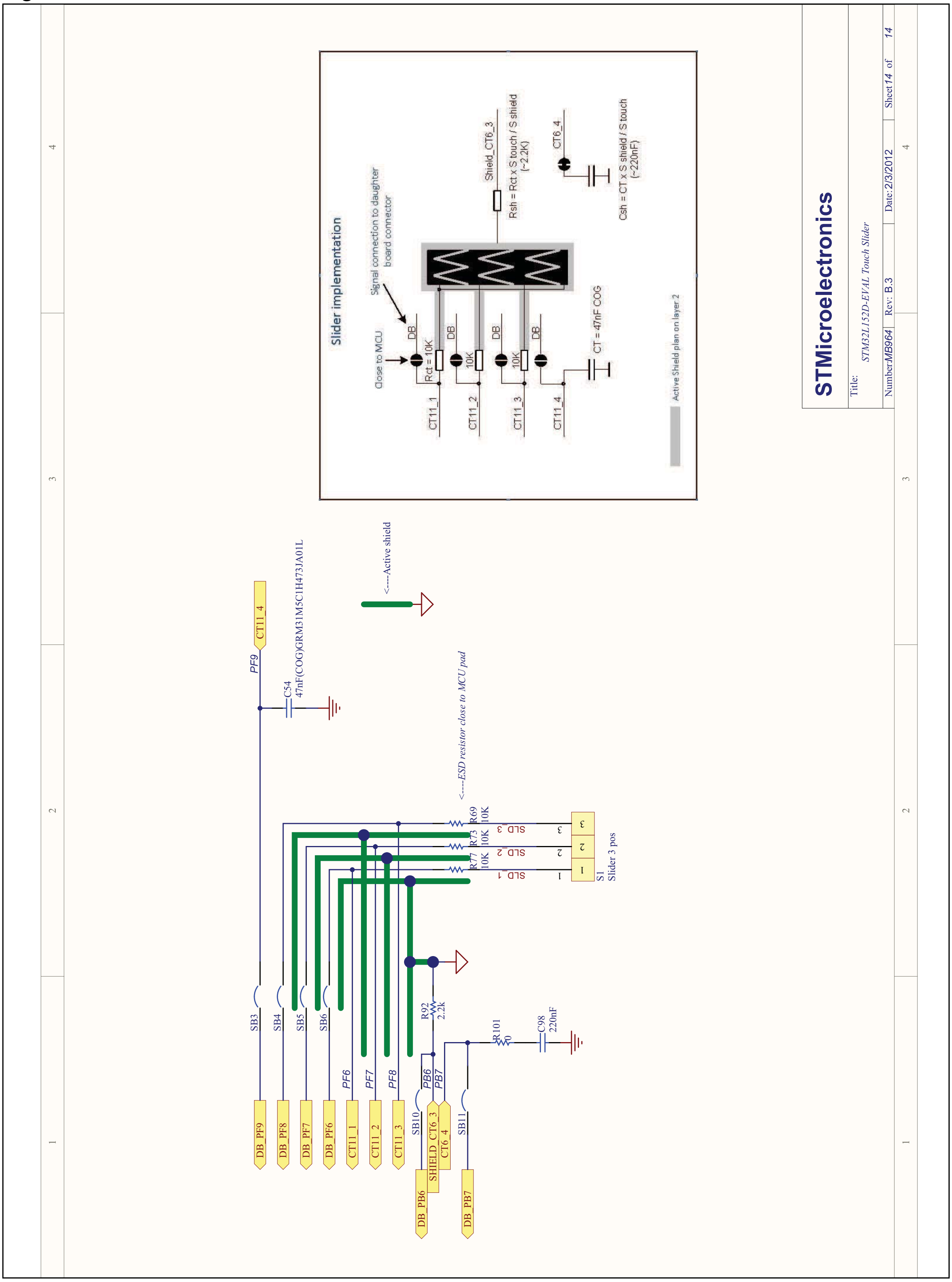


Figure 34. LCD glass daughter board MB979

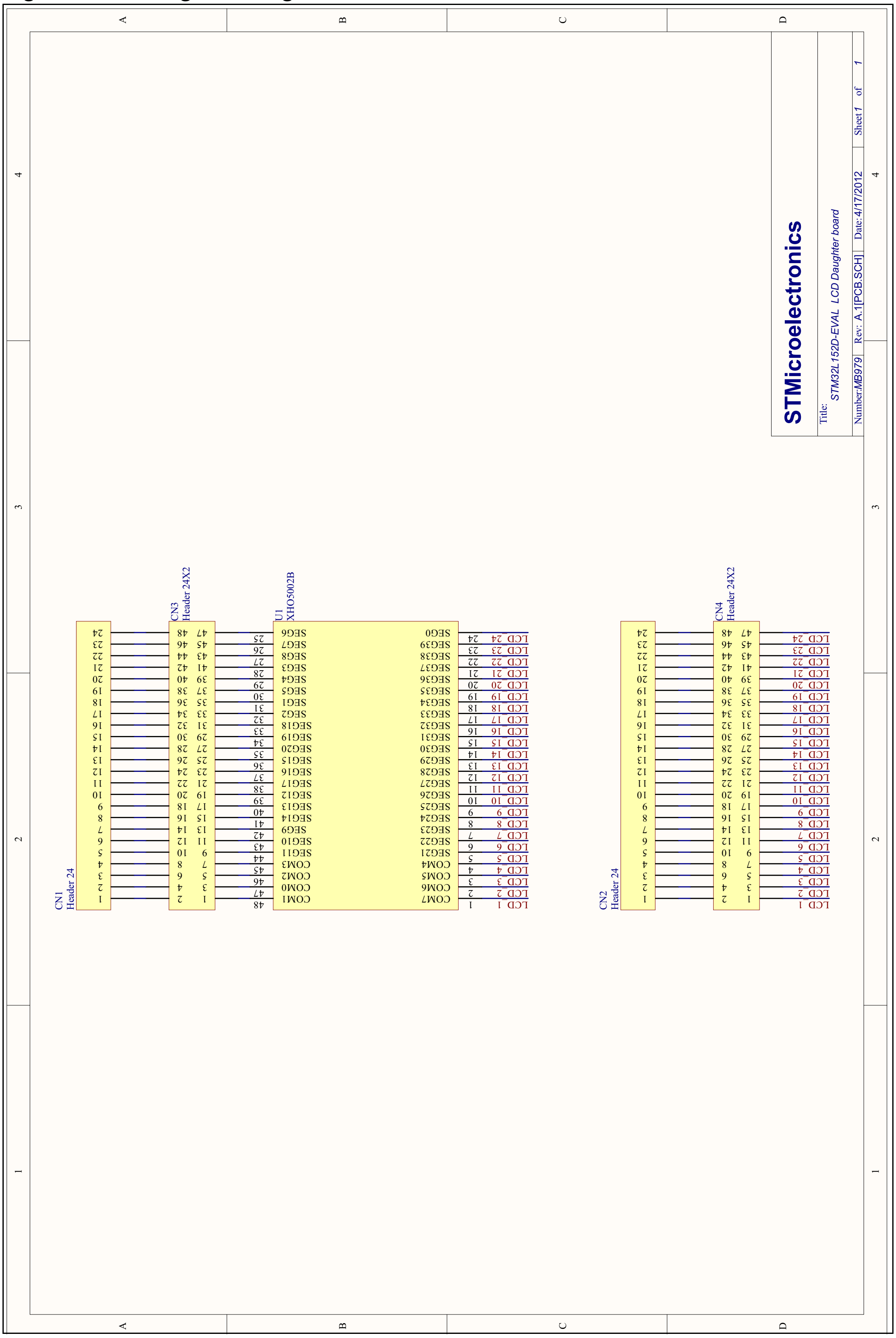
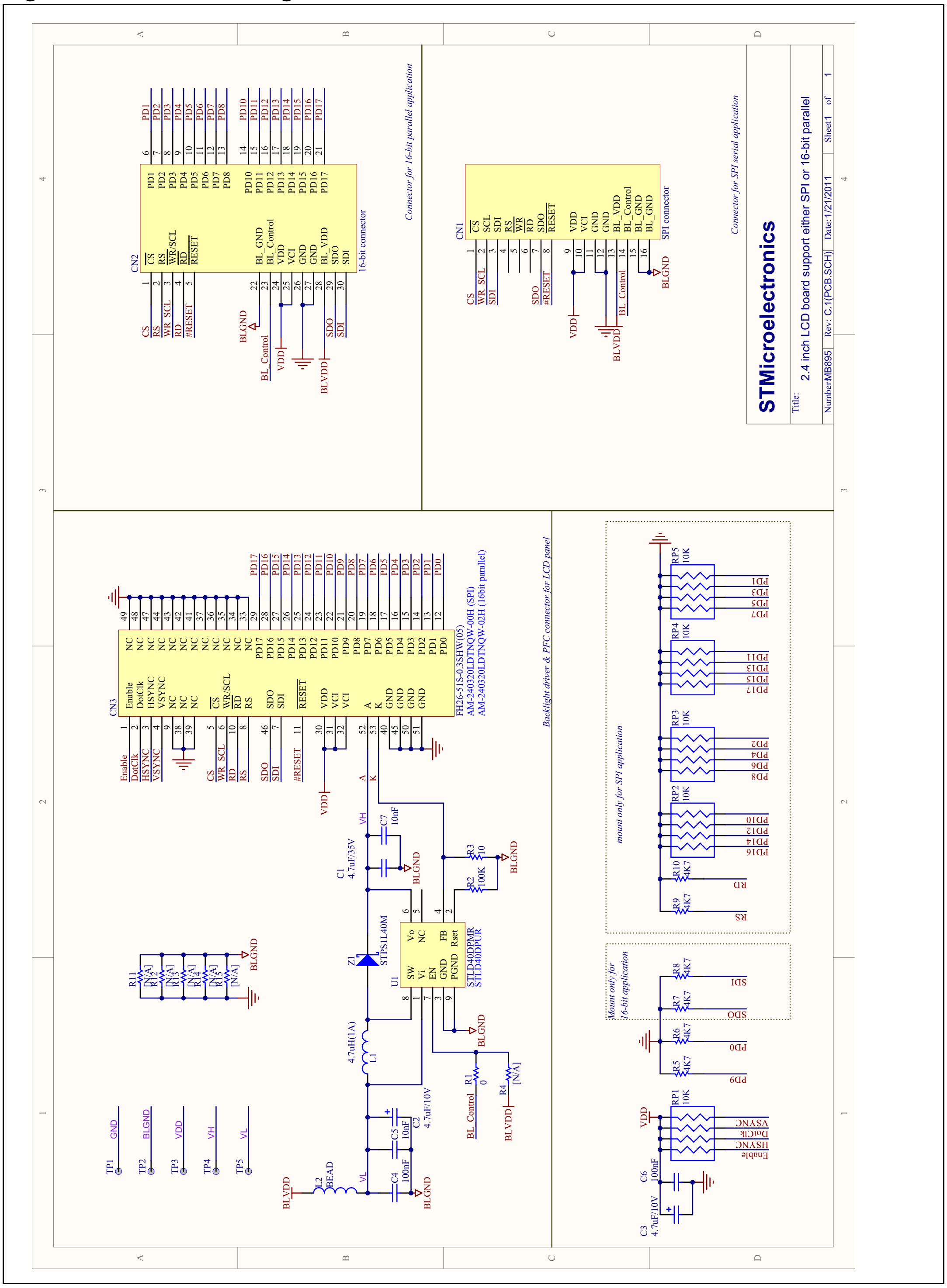


Figure 35. TFT LCD daughter board MB895



Appendix A STM32L152D-EVAL I/O assignment

Table 34. STM32L152D-EVAL I/O assignment

Pin No.	Pin name	STM32L152D-EVAL I/O assignment
1	PE2	SEG 38 / A23 / TRACECK
2	PE3	SEG 39 / A19 / TRACED0
3	PE4	A20 / TRACED1
4	PE5	A21 / TRACED2
5	PE6	TAMPER3/TRACED3 / WKUP3/U5V_DET
6	VLCD	V_LCD
7	PC13ANTI_TAMP	IDD_CNT_EN
8	PC14OSC32_IN	OSC32_IN
9	PC15OSC32_OUT	OSC32_OUT
10	PF0	A0
11	PF1	A1
12	PF2	A2
13	PF3	A3
14	PF4	A4
15	PF5	A5
16	VSS_5	GND
17	VDD_5	VDD
18	PF6	SLIDER_CT_11_1
19	PF7	SLIDER_CT_11_2
20	PF8	SLIDER_CT_11_3
21	PF9	SLIDER_CT_11_4
22	PF10	POTENTIOMETER_ADC31
23	PH0OSC_IN	OSC_IN
24	PH1OSC_OUT	OSC_OUT
25	NRST	NRST
26	PC0	SEG18
27	PC1	SEG19 / LPF_OA3_INP
28	PC2	SEG20
29	PC3	SEG21 / LPF_OA3_OUT
30	VSSA	GND
31	VREF-	GND
32	VREF+	VDDA

Table 34. STM32L152D-EVAL I/O assignment (continued)

Pin No.	Pin name	STM32L152D-EVAL I/O assignment
33	VDDA	VDDA
34	PA0WKUP	IDD_WAKEUP / KEY_TAMPER2/WKUP1
35	PA1	SEG0 / Micro_OA1_INP
36	PA2	SEG1 / Micro_OA1_INN
37	PA3	SEG2 / Micro_OA1_OUT
38	VSS_4	GND
39	VDD_4	VDD
40	PA4	CON_ADC4 -DAC1 / Audio_DAC_OUT
41	PA5	E2P_SCK
42	PA6	SEG3 / ADJ_G_OA2_INP
43	PA7	SEG4 / ADJ_G_OA2_INN
44	PC4	SEG22
45	PC5	SEG23 / E2P_CS
46	PB0	SEG5 / ADJ_G_OA2_OUT
47	PB1	SEG6 / Audio_DAC_RST
48	PB2	BOOT1
49	PF11	IDD_ADC_IN1b
50	PF12	A6
51	VSS_6	GND
52	VDD_6	VDD
53	PF13	A7
54	PF14	A8
55	PF15	A9
56	PG0	A10
57	PG1	A11
58	PE7	D4
59	PE8	D5
60	PE9	D6
61	VSS_7	GND
62	VDD_7	VDD
63	PE10	D7
64	PE11	D8
65	PE12	D9
66	PE13	D10
67	PE14	D11 / E2P_ MISO

Table 34. STM32L152D-EVAL I/O assignment (continued)

Pin No.	Pin name	STM32L152D-EVAL I/O assignment
68	PE15	D12 / E2P_ MOSI
69	PB10	SEG10
70	PB11	SEG11
71	VSS_1	GND
72	VDD_1	VDD
73	PB12	SEG12 / I2S2_WS
74	PB13	SEG13 / I2S2_CK
75	PB14	SEG14
76	PB15	SEG15 / I2S2_SD
77	PD8	SEG28 / D13
78	PD9	SEG29 / D14
79	PD10	SEG30 / D15
80	PD11	SEG31 / A16
81	PD12	SEG32 / A17
82	PD13	SEG33 / A18
83	VSS_8	GND
84	VDD_8	VDD
85	PD14	SEG34 / D0
86	PD15	SEG35 / D1
87	PG2	A12
88	PG3	A13
89	PG4	A14
90	PG5	A15
91	PG6	JOYSTICK_LEFT
92	PG7	JOYSTICK_RIGHT
93	PG8	JOYSTICK_DOWN
94	VSS_9	GND
95	VDD_9	VDD
96	PC6	SEG24 / I2S2_MCK
97	PC7	SEG25 /uSD_DET
98	PC8	SEG26 / uSD_D0
99	PC9	SEG27 / uSD_D1
100	PA8	COM0
101	PA9	COM1 / USART1_TX
102	PA10	COM2 / USART1_RX

Table 34. STM32L152D-EVAL I/O assignment (continued)

Pin No.	Pin name	STM32L152D-EVAL I/O assignment
103	PA11	USB_DM
104	PA12	USB_DP
105	PA13	JTMSSWDAT
106	PH2	A22
107	VSS_2	GND
108	VDD_2	VDD
109	PA14	JTCKSWCLK
110	PA15	SEG17 / JTDI
111	PC10	COM4 / SEG28/ SEG40 / uSD_D2
112	PC11	COM5 / SEG29 /SEG41 / uSD_D3
113	PC12	COM6 / SEG30 / SEG42 / uSD_CK
114	PD0	D2
115	PD1	D3
116	PD2	COM7 / SEG31 / SEG43 / uSD_CMD
117	PD3	LED1
118	PD4	OEN
119	PD5	WEN
120	VSS_10	GND
121	VDD_10	VDD
122	PD6	WAITN
123	PD7	LED2
124	PG9	CS_NOR_EBAR1
125	PG10	CS_RAM_EBAR2
126	PG11	JOYSTICK_UP
127	PG12	LCD_EBAR3
128	PG13	JOYSTICK_SELECT
129	PG14	LED3
130	VSS_11	GND
131	VDD_11	VDD
132	PG15	LED4
133	PB3	SEG7 / POT_COMP_INN / JTDO/SWO
134	PB4	SEG8 / LDR_COMP_INP / JTRST
135	PB5	SEG9 / POT_COMP_INP / Temp_SMBAI
136	PB6	Shield_CT_6_3
137	PB7	C_Shield_CT_6_4

Table 34. STM32L152D-EVAL I/O assignment (continued)

Pin No.	Pin name	STM32L152D-EVAL I/O assignment
138	BOOT0	BOOT0
139	PB8	SEG16 / AUDIO_RF_Temp_SCL
140	PB9	COM3 / AUDIO_RF_Temp_SDA
141	PE0	SEG36 / BLN0
142	PE1	SEG37 / BLN1
143	VSS_3	GND
144	VDD_3	VDD

Appendix B Mechanical dimensions

Figure 36. Mechanical dimension

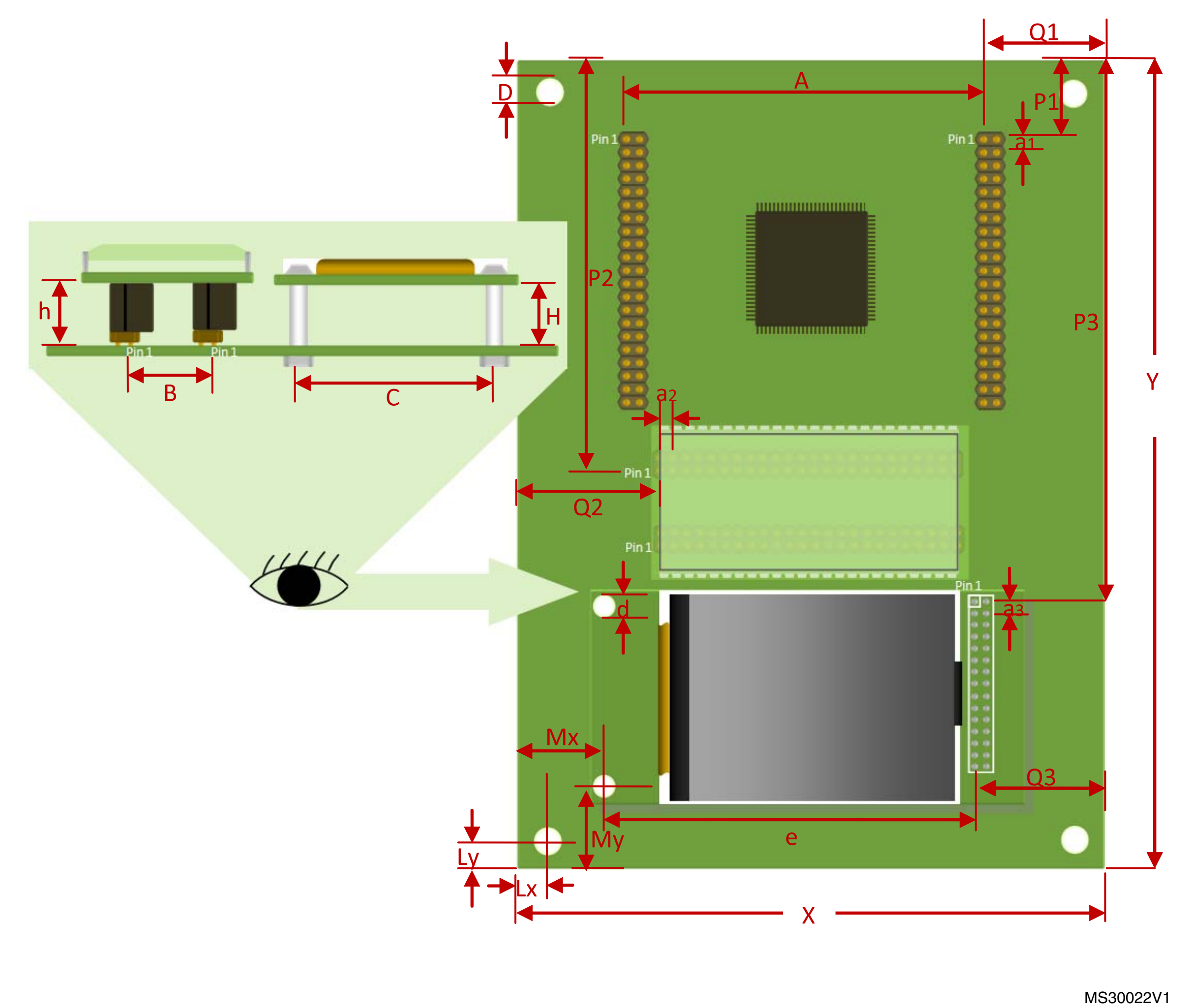


Table 35. Mechanical dimensions

Symbol	Size (mm)	Symbol	Size (mm)	Symbol	Size (mm)
A	68.58	e	72.363	P2	84.455
a1	2.54	H	11	P3	115.247
a2	2.54	h	12	Q1	24.13
a3	2.54	Lx	5.715	Q2	26.67
B	17.78	Ly	5.715	Q3	24.792
C	36	Mx	17.145	X	114.3
D	3.5	My	20.32	Y	172.72
d	3.2	P1	18.415		

Revision history

Table 36. Document revision history

Date	Revision	Changes
30-Mar-2012	1	Initial release.
03-Jul-2012	2	Updated *Section 2.19: Display and input devices* and added *Table 21*. Added *Table 1: Applicable products*, *Figure 34: LCD glass daughter board MB979* and *Figure 35: TFT LCD daughter board MB895*. Added note in *Section 2.18: Temperature sensor*.